ME Electronics (VLSI Design)

Course Name	:	ELECTRONIC SYSTEM DESIGN
Course Code	:	EVN 511
Credits	:	3
L T P	:	3 0 0

Course Objectives :

Course Objective: This subject covers the basics of digital logic circuits and design. Through the basic understanding of Boolean Algebra and Number systems , it introduces the student to the fundamentals of combination logic design and then to sequential circuits(both synchronous and asynchronous). Memory systems are also covered. There is an introduction to VHDL. Students will be provided with an opportunity to implement the PLD based designs(using both schematic capture and VHDL) in actual chips.

Total no. of lectures (42)

Lecture wise Break Up		No. of Lectures
1	DESIGN CONCEPTS Digital Hardware, Design Process, Design of Digital Hardware	(02)
2	LOGIC CIRCUITS Variables & Functions, Logic gates & Networks synthesis, Introduction to VHDL.	(03)
3	OPTIMIZED IMPLEMENTATION OF LOGIC FUNCTIONS: Strategy for minimization, Incompletely specified functions, Multiple output circuits, Multilevel synthesis & Analysis.	(06)
4	COMBINATIONAL CIRCUITS Building Block, Multiplexers Decoders, Encoders Code Converters and their implementation in VHDL.	(06)
5	SYNCHRONOUS SEQUENTIAL CIRCUITS Basic Design Steps, Mealy state Model, Design of FSM and their implementation using VHDL programming.	(09)
6	ASYNCHRONOUS SEQUENTIAL CIRCUITS Analysis, Synthesis, State Reduction, State Assignment, Hazards.	(08)
7	DIGITAL SYSTEM DESIGN Building Block Circuits.	(04)
8	TESTING OF LOGIC CIRCUITS Fault Model, Path sensitizing, Random testing, Circuits with Tree Structure.	(04)

Course Outcome :		
1	The students will be able to design, simulate , built and debug complex combinational and sequential circuits based on an abstract functional specification.	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of publication / Reprint
Text Books 1	Introduction to Logic Design – MARCOVITZ – (Text)	3rd Ed 2009
Reference 1	A VHDL Primer- Bhaskar	3rd Ed 1998
2	An Engineering Approach to Digital Design - FLETCHER	1997
3	Logic and Computer Design Fundamentals – MANO	5th Ed 2015

Course Name	:	MICROELECTRONICS
Course Code	:	EVN 512
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
As part of this course, students will understand the physical, electrical, and optical properties of semiconductor materials and their use in microelectronic circuits. Relate the atomic and physical properties of semiconductor materials to device and circuit performance issues. Develop an understanding of the connection between device-level and circuit-level performance of microelectronic systems.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	MICROELECTRONICS TECHNOLOGY Introduction and its use in I.C. fabrication. Scales of integration from SSI to ULSI. Stages of Manufacturing, Process and product trends, Wafer preparation, process yields.	(02)
2	CRYSTAL GROWTH (02) Single Crystal growth of Silicon and Gallium Arsenide. Substroth slicing and polishing. Zen refining of Semiconductor crystals.	(02)
3	SEMICONDUCTOR MATERIAL PREPERATION (02) Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction Oxidation and Photolithography	(02)
4	OXIDATION Oxide layer growth on Silicon wafer surface. Oxidation in the presence of dry oxygen & wet oxygen. Oxide layer growth along various crystal directions.	(04)

5	DIFFUSION Solution to Fick's Laws Junction formation. Diodes, transistors and MOSFETs.	(04)
6	EPITAXY VPE, LPE and MBE: Individual epitaxial units, their operation and quality of film growth.	(05)
7	ION IMPLANTATION The process and techniques for formation of ion-implanted doped layers and their characteristics.	(04)
8	THIN FILM DEPOSITION Growth of thin metallic films. Normal and ultra-high vacuum systems. Thickness monitors.	(04)
9	CHEMICAL VAPOUR DEPOSITION Growth of CVD films. Growth mechanism and characterization. MOCVD	(04)
10	STANDARD BIPOLAR, NMOS AND CMOS CIRCUITS Processing and fabrication using circuit layout. Process evaluation.	(04)
11	SI-MOS CAPACITOR Its fabrication and characteristics.	(02)
12	SUB MICRON DEVICE PHYSICS AND TECHNOLOGY Review of basic device physics, MOS capacitor and transistor theory, Moore's law on technology scaling, MOS device scaling theory, Short channel effects, sub threshold leakage, Punch through, DIBL, High field mobility, Velocity saturation and overshoot, ULSI technology, Nano fabrication	(05)

Course Outcomes - Upon successful completion of this course, students should be able to: .		
1	Compute carrier concentrations for semiconductor materials under a variety of conditions.	
2	Compute conductivity and resistivity of semiconductor materials under a variety of conditions	
3	Compute terminal voltage and current characteristics for pn junction diodes under a variety of conditions.	
4	Compute terminal voltage and current characteristics for bipolar transistors under a variety of conditions.	
5	Compute terminal voltage and current characteristics for MOS transistors under a variety of conditions	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books	S.M. Sze, G.May, Fundamental of Semiconductor Fabrication	2007
Reference :1	Peter Van Zant, Microchip Fabrication, 5th Edition, McGraw-Hill.	2004
2	C.Y. Chang and S.M.Sze, ULSI Technology, McGraw-Hill.	2000
3	Eugene D.Fabricius, Introduction to VLSI Design, McGraw-Hill.	1990
4	Microelectronics: Theory Design and Fabrication by Edward Keonjian.	1963
5	Microelectronics –Jacob Millman	1987

Course Name	:	DIGITAL VLSI DESIGN
Course Code	:	EVN 513
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
The course objective is to introduce the fundamental principles of VLSI circuit design and to examine the basic building blocks of large-scale digital integrated circuits.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Physics and Modeling of MOSFETs Basic MOSFET Characteristics – Threshold Voltage, Body Bias concept, Current-Voltage Characteristics – Square-Law Model, MOSFET Modeling – Drain-Source Resistance, MOSFET Capacitances, Geometric Scaling Theory – Full-Voltage Scaling, Constant-Voltage Scaling. Trends and Limitations of CMOS , Challenges of MOSFET Scaling.	(06)
2	Fabrication and Layout of CMOS Integrated Circuits Overview of Integrated Circuit, Processing – Oxidation, Photolithography, Self-Aligned MOSFET, Isolation and Wells – LOCOS, Trench Isolation, CMOS Process flow, Mask design and Layout – MOSFET ,Dimensions, Design Rules, Latch-up.	(05)

3	CMOS Inverter Basic Circuit and DC Operation – DC Characteristics, Noise Margins, Layout considerations, Inverter Switching Characteristics – Switching Intervals, High-to-Low time, Low-to-High time, Maximum Switching Frequency, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance, Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads.	(05)
4	Switching Properties of MOSFETs nMOSFET/ MOSFET Pass Transistors, Transmission Gate Characteristics, MOSFET Switch Logic, TG-based Switch Logic, D-type Flip-Flop.	(04)
5	Static CMOS Logic Elements Complex Logic Functions, CMOS NAND Gate, CMOS NOR Gate, Complex Logic Gates, Exclusive OR and Equivalence Gates, Adder Circuits, Pseudo-nMOS Logic Gates, Schmitt Trigger Circuits, SR and D-type Latch, CMOS SRAM Cell, Tri-state Output Circuits.	(05)
6	Power Dissipation in CMOS Digital Circuits Dynamic Power Dissipation – Switching Power, Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Static Power, Dissipation – Diode Leakage Current, Sub-threshold Leakage Current.	(04)
7	Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families, Charge Leakage, Charge Sharing, Dynamic RAM Cell, Bootstrapping, Clocked-CMOS, Pre- Charge/ Evaluate, Logic, Domino Logic, Multiple-Output Domino Logic, NORA Logic, Single-Phase Logic.	(05)
8	CMOS Differential Logic Styles Dual-Rail Logic, CVSL, CPL, DPL, DCVS, MCML	(04)
9	Issues in Chip Design ESD Protection, On-Chip Interconnects – Line Parasitics, Modeling of the Interconnect Line, Clock Distribution, Input-Output circuits.	(04)

Course Outcomes :		
1	The students will be able to design logic circuit layouts for both static CMOS and dynamic clocked CMOS circuits, to extract the analog parasitic elements from the layout and analyze the circuit timing using a logic simulator and an analog simulator, to insert elementary testing hardware into the VLSI chip, to analyze VLSI circuit timing using Logical Effort analysis and to estimate and compute the power consumption of a VLSI chip	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books	Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill	3rd Ed 2008
2 References	Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, Addision Wesley	2nd Ed 1998
3	Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits – A Design Perspective, Pearson Education	2nd Ed 2007
4	aker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley - IEEE Press	2nd Ed 2004
5	Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley	3rd Ed 2006

Course Name	:	LOW POWER DESIGN TECHNIQUES
Course Code	:	EVN 514
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
To study the concepts on different levels of power estimation and optimization techniques. For today´s electronic devices, low-power dissipation is desirable; for mobile, battery-operated applications, power is the tightest design constraint. An integrated framework for low-power design of digital systems must provide the user with methods and tools for power optimization at all stages of the design development flow (i.e., from system specification to implementation). This course provides the students with an exhaustive review of state-of-the-art techniques for power estimation and optimization of digital VLSI systems. Both dynamic and static (i.e., leakage) power are considered, and the problems of modeling, estimation and optimization of power consumption are addressed at different levels of abstraction. Lab sessions will introduce the students to the usage of some of the most popular tools for low-power design.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Introduction Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Estimation of power dissipation due to switching, short circuit, sub-threshold leakage, and diode leakage currents.	(04)
2	Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness,	(07)

	Impact of technology Scaling, Technology & Device innovation	
3	Low Voltage Technologies and Circuits Threshold Voltage Scaling and Control, Multiple Threshold CMOS (MTCMOS), Substrate Bias Controlled Variable Threshold CMOS, Testing Issues: Design and test of low-voltage CMOS circuits.	(08)
4	Circuit and Logic Styles Power-conscious logic Styles, Adiabatic Logic Circuits. Power Analysis and optimization: Power Analysis Techniques, Power Optimization Techniques, Energy recovery techniques, Software power estimation and optimization Low-Power Memory Circuits and architectures.	(06)
5	Low power Architecture & Systems Power & performance management, switching activity reduction, parallel architecture with voltage reduction, low power arithmetic components, low power low voltage adder design approaches, multiplier design approaches and low power memory design	(08)
6	Power Conscious High-Level Synthesis	(05)
7	Silicon-On-Insulator Based Technologies	(04)

Course Outcomes : To design chips used for battery-powered systems and high-performance circuits not exceeding power limits.		
1	Be able to use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnect.	
2	Be able to create models of moderately sized CMOS circuits that realize specified digital functions.	
3	Be able to apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.	
4	Identify the sources of power dissipation in digital IC systems. Understand the impact of power on system performance and reliability.	
5	Characterize and model power consumption. Understand the basic analysis methods	
6	Understand the voltage scaling approaches for different design abstraction levels.	
7	Apply probabilistic analysis to characterize dynamic power estimation.	
8	Understand leakage sources and reduction techniques	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books:	Roy, K. and Prasad, Sharat C., Low Power CMOS VLSI: Circuit Design, John Wiley.	2009
1 Reference Books:	Rabaey, J.M., Low Power Design Essentials, Springer	2009
2	Kiat-Seng Yeo, Roy K., Low voltage Low power VLSI subsystems, Tata Mcgraw-Hill	2009
3	Chandrakasan, A.P. and Broderson, R.W., Low Power Digital CMOS Design, Kluwer	1995
4	Rabaey, J.M. and Pedram, M., Low Power Design Methodologies, Springer	1996
5	Bellaouar, A. and Elmasry, M.I., Low-Power Digital VLSI Design : Circuits and Systems, Kluwer	1995

Course Name	:	REAL TIME SYSTEMS
Course Code	:	EVN 515
Credits	:	3
L T P	:	3 0 0

Course Objectives :

Knowledge

The student has an understanding of and practical experience with real-time systems.
The student has an understanding of Adaptive Filtering.
The student has an understanding of Digital Signal Processors.

Skills

The student should be able to judge the arithmetic complexity of various algorithms and choose suitable real-time hardware, write program code, debug and test algorithm in real time.

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Introduction: Definition, Issues in Real Time Computing, Structure of a Real Time System. Task Classes	(04)
2	Characterizing Real Time Systems and Tasks: Introduction, Performance measures for real time systems: Traditional performance measures, Performability, Cost functions and hard Deadlines	(09)
3	Task Assignment and Scheduling: Introduction, Classical Uniprocessor scheduling algorithms: Rate Monotonic, EDF algorithm, Task assignment, Fault tolerant Scheduling	(10)

4	Real Time Databases: Basic definitions, Real time Vs General Purpose databases, Main Memory databases, concurrency control issues, databases for hard real time systems	(10)
5	Real Time Communication: Introduction, Architectural Issues, Protocols: Contention based protocols, Token based protocols, Deadlines based protocols, Stop and Go Multichip protocol, The polled bus protocol, Hierarchical round robin protocol.	(09)

Course Outcomes :		
1	Understand the basics and importance of real-time systems	
2	Generate a high-level analysis document based on requirements specifications	
3	Generate a high-level design document based on analysis documentation	
4	Generate a test plan based on requirements specification	
5	Generate a validation plan based on all documentation	
6	Understand basic multi-task scheduling algorithms for periodic, aperiodic, and sporadic tasks as well as understand the impact of the latter two on scheduling	

Course Name	:	DESIGN OF SEMICONDUCTOR MEMORIES
Course Code	:	EVN 516
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
Different memory devices like, RAM, ROM, PROM, EPROM, EEPROM, etc. Different terms like: read, write, access time, nibble, byte, bus, word, word length, address, volatile, non-volatile etc. How to implement combinational and sequential circuits using ROM.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	RANDOM ACCESS MEMORY TECHNOLOGIES: Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM, Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon on Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.	(09)

2	NONVOLATILE MEMORIES: Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) – Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture- Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture. (08)	(08)
3	MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE: RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.	(08)
4	RELIABILITY AND RADIATION EFFECTS: General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Qualification. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.	(09)
5	PACKAGING TECHNOLOGIES: Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dissymmetry-Water Level Radiation Testing and Test Structures. Random Access Memories.	(08)

Course Outcomes :		
1	Describe the technology used in the construction of digital memory, and assess the quality of various memory types. Draw the schematic of a static and dynamic memory cell and explain in details the process of reading and writing a bit of information in it. Draw the schematic of a typical sense amplifier and explain how it works. Draw a schematic of a simple (2-3 bit) NOR/NAND NMOS address decoder and explain how it decodes a given address.	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books	Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of India Private Limited, New Delhi,	1997
1 Reference Books:	Tegze P.Haraszti, "CMOS Memory Circuits", Kluwer Academic publishers	2001
2	Betty Prince, "Emerging Memories: Technologies and Trends", Kluwer Academic publishers, 2002.	2002

Course Name	:	ANALOG CMOS DESIGN
Course Code	:	EVN 517
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
This course introduces the principles of analog and mixed-signal IC design in CMOS technologies. Design and analysis of fundamental building blocks and basic analog circuits are covered to provide a foundation for more complicated and advanced designs, some of which we will touch on. Both practical design and layout issues will be emphasized. One challenging project will be assigned to be worked on in groups.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Basic MOS Device Physics: MOS IV Characteristics, Second order effects, Short-Channel Effects, MOS Device Models, Review of Small Signal MOS Transistor Models, and MOSFET Noise. (7)	(07)
2	Analog MOS Process: Analog CMOS Process (Double Poly Process), Digital CMOS Process tailored to Analog IC fabrication, Fabrication of active devices, passive devices and interconnects, Analog Layout Techniques, Symmetry, Multi-finger transistors.	(07)
3	Passive devices: Capacitors and Resistors, Substrate Coupling, Ground Bounce. Single Stage Amplifiers: Common Source Stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode.	(05)
4	Differential Amplifier: Single ended and Differential Operation, Qualitative and Quantitative Analysis of Differential pair, Common	(05)

	Mode response, Gilbert Cell.	
5	Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.	(04)
6	Feedback: General Considerations, Topologies, Effect of Loading.	(02)
7	Operational Amplifier: General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR.	(07)
8	Stability and Frequency Compensation: General Considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation Techniques.	(05)
Course Outcomes :		
1	The student must at the end of the course be able to understand the operation of CMOS devices, familiar with the small- and large-signal models of CMOS transistors, analyze the basic current mirrors, understanding the voltage references, analyze and design basic operational amplifiers, understand the concept of gain, power, and bandwidth, design basic circuits using EDA tools	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books	Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill.	2008
2 References	Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley.	2004
3	Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press.	2nd Ed 2002
4	Johns, D.A. and Martin, K., Analog Integrated Circuit Design, John Wiley.	2008
5	Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley.	5th Ed 2001
6	Hastings, A., The Art of Analog Layout, Prentice Hall	2005

Course Name	:	COMPUTER AIDED VLSI DESIGN
Course Code	:	EVN 520
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
To provide an introduction to the fundamentals of Computer-Aided Design tools for the modelling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Hardware Description languages, Verifying behavior prior to system construction simulation and logic verification, Logic synthesis	(13)
2	PLA based synthesis and multilevel logic synthesis, logic optimization, Logic simulation, compiled and event simulators, relative advantages and disadvantages.	(11)
3	Layout Algorithms Circuit partitioning, placement, and routing algorithms; Design rule verification; Circuit Compaction; Circuit extraction and post layout simulation	(09)
4	Automatic Test Program Generation; Combinational testing D-Algorithm and PODEM algorithm; Scan-based testing of sequential circuits; Testability measures for circuits.	(09)

Course Outcomes :		
1	Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification. Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books	N.A. Sherwani, " Algorithms for VLSI Physical Design Automation ".	1999
2	S.H. Gerez, " Algorithms for VLSI Design Automation ", 1998.4. J. Bhasker, "A VHDL Primer", Addison-Weseley Longman Singapore Pte Ltd.	1992

3	Drechsler, R., *Evolutionary Algorithms for VLSI CAD*, Kluwer Academic Publishers, Boston, 1998.	1998
4	Verilog HDL by Samir Palnitkar	
1 Reference Books	VERILOG HDL SYNTHESIS: A PRACTICAL PRIMER by J Bhaskar	1998
2	Hill, D., D. Shugard, J. Fishburn and K. Keutzer, *Algorithms and Techniques for VLSI Layout Synthesis*, Kluwer Academic Publishers, Boston	1989

Course Name	:	TESTING & FAULT TOLERANCE
Course Code	:	EVN 521
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
To provide students with an understanding of fault tolerant computers, including both the theor of how to design and evaluate them and the practical knowledge of real fault tolerant systems.		

Total No. of Lectures: (42)

Lecture wise Break Up		No. of Lectures
1	Deductive, Parallel, and Concurrent Fault Simulation, Critical Path Tracing	(07)
2	ATPG for Combinational Circuits: D- Algorithm, Boolean difference, Podem, Random, Deterministic and Weighted Random Test Pattern Generation Aliasing and its Effect on Fault Coverage.	(09)
3	PLA Testing, Cross Point Fault Model and Test Generation, Memory Testing - Permanent, Intermittent and Pattern Sensitive Faults, Marching, Tests, Delay Faults.	(09)
4	ATPG for Sequential Circuits, Time Frame, Expansion; Controllability and Observability Scan Design, BILBO, Boundary Scan for Board Level Testing, BIST and Totally Self checking Circuits, System level Diagnosis.	(09)
5	Introduction, Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes, Reconfiguration Techniques, Yield Modelling Reliability and effective area utilization.	(08)

Course Outcomes :		
1	The students will be able to analyze a system for performance-dependability tradeoffs and to select the appropriate points in an end-to-end system to embed fault-tolerant techniques	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 TextBooks	Abramovici, M., Breuer, M. A. and Friedman, A.D., Digital Systems Testing and Testable Design Jaico Publishing House.	2001
1Reference Books	Bushnell, M. and Agrawal, V.D., Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits, Kluwer Academic.	2000
2	Pradhan, D.K., Fault Tolerant Computer System Design, Prentice Hall.	1996
3	Slewiorek, D.P., Swarz, R. S. and Peters A.K., Reliable Computer Systems:Design and Evaluation, A K Peters 3rd ed.	1998

Course Name	:	EMBEDDED SYSTEMS
Course Code	:	EVN 522
Credits	:	3
L T P	:	3 0 0

Course Objectives :

1. Describe what makes a system a real-time system.
2. Explain the presence of and describe the characteristics of latency in real-time systems.
3. Summarize special concerns that real-time systems present and how these concerns are addressed.

Total No. of Lectures: 42

Lecture wise Break Up		No. of Lectures
1	Embedded Processing: Introduction to Embedded Computing, Difference between Embedded and General-Purpose Computing, Characterizing Embedded Computing, Design Philosophies, RISC, CISC, VLIW versus superscalar, VLIW versus DSP Processors, Register File Design, Pipeline Design, the control unit, control registers.	(10)
2	Embedded Processors: Microprocessor versus Microcontroller architecture, ARM architecture, Assembly Programming, Input-Output interfacing, GPIO, LCD interfacing, Peripherals, DDR Memory, SDRAM, interrupts, Timers.	(07)
3	Atom Processor, Architecture, Application Development Tools (Hands on Experience on Atom Boards)	(06)
4	RTOS and Application design: Real time operating systems, Embedded	(10)

	RTOS, Real time process scheduling, structure of real time, operating system, Memory management in Embedded operating system, operating system, overhead, interprocess communication mechanisms, File systems in Embedded devices, Different, types of locks, Semaphores, Application studies with Vxworks, Linux etc.	
5	System Design & Simulation: System-on-a-Chip (SoC), IP Blocks and Design Reuse, Processor Cores and SoC, Non-programmable accelerators, reconfigurable logic, multiprocessing on a chip, symmetric multiprocessing, heterogeneous multiprocessing, In Circuit Emulation, Validation and verification, H/W Software partitioning, Co-design.	(09)

Course Outcomes :		
1	Upon completion of this course, the student will be able to: 1. Understand and design embedded systems and real-time systems For real-time systems: • Identify the unique characteristics of real-time systems • Explain the general structure of a real-time system • Define the unique design problems and challenges of real-time systems • Apply real-time systems design techniques to various software programs.	
2	2 For embedded systems it will enable you to : • Understand the basics of an embedded system • Program an embedded system • Design, implement and test an embedded system. • Ex: realtime + embedded : games on a Gameboy or arcade games Ex: realtime: Spore on a laptop	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Book	Wolf, W., High-Performance Embedded Computing Architectures, Applications, and Methodologies, Morgan Kaufman Publishers.	2007
1Reference Books:	Heath, S., Embedded Systems Design, Elsevier Science.	2003
2	Fisher, J.A., Faraboschi, P. and Young, C., Embedded	2005

	Computing - A VLIW Approach to Architecture, Compilers and Tools, Morgan Kaufman.	
3	Simon, D.E., An Embedded Software Primer, Dorling Kindersley.	2005
4	Lori Matassa, Max Domeika, Break Away with Intel Atom Processors: A Guide to Architecture Migration, Intel Press (December 16).	2010
5	Andrew Sloss, Dominic Symes, Chris Wright, ARM System Developer's Guide: Designing and Optimizing System Software, Morgan Kaufmann, Elsevier.	2004

Course Name	:	ADVANCED DIGITAL SIGNAL PROCESSING
Course Code	:	EVN 523
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
The purpose of this course is to provide in-depth treatment on methods and techniques in discrete-time signal transforms, digital filter design, optimal filtering, power spectrum estimation, multi-rate digital signal processing, DSP architectures, which are of importance in the areas of signal processing, control and communications.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	DIGITAL FILTERS: FIR filters, IIR filters. Digital filter design techniques: Impulse invariance. Bilinear transformation, finite difference, window design methods, frequency sampling optimization algorithms. MATLAB problems.	(05)
2	Wavelet Transform : Continuous & discrete wavelet transforms, Filter Banks. MATLAB problems, STFT (discreet and continuous time)	(04)
3	Effects of finite word length in DSP system : Rounding and truncation errors, quantization effects in A/D converter, FIR and IIR filters	(04)
4	Multi-rate Signal Processing : Integer sampling rate conversion. Interpolation and decimation filters. Design of practical sampling rate converters. Sampling rate conversion by an arbitrary factor. Applications of multi-rate signal processing in telecommunications.	(05)
5	Adaptive Filtering : Concepts, Adaptive filters as noise cancellers, adaptive line enhancer, in-system modeling. Basic Wiener filter.	(04)
6	Linear Prediction :	(04)
7	Applications of DSP : Radar, sonar, biomedical, communications,	(04)

	speech and image processing.	
8	Adaptive Signal Processing	(04)
9	Basic Concepts of Speech Signal Processing	(04)
10	Power Spectrum Estimation	(04)

Course Outcomes :		
1	The topics covered in this course provide comprehensive foundation for other more specialized areas in signal processing, control, and communications. At the end of the course, students would be able to apply fundamental principles, methodologies and techniques of the course to analyze and design various problems encountered.	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Textbook:	Digital Signal Processing-E C Ifeacher& B W Jervis; PHI	2002
2 REFERENCES:	Digital Signal Processing-A.V. Oppenheim & B.W. Jervis; PHI.	2006
3	Digital Signal Processing-J.G. Prokis& D.G. Manolakis; PHI.	4th Ed 2006
4	Digital Signal Processing-M.H. Hayes; Schaum's Outlines.	2nd Ed 2011
5	Digital Signal Processing-S Salivahanan, AVallavraj& C Gyanapriya; TMH.	2nd Ed 2011
6	Applied Digital signal processing – Manolakis, Ingle	2011

Course Name	:	FPGA BASED SYSTEM DESIGN
Course Code	:	EVN 524
Credits	:	3
L T P	:	3 0 0

Course Objectives :

The goal is to enable students to design and implement custom computing systems with FPGAs. Students will gain knowledge and understanding of

- Different technologies to implement digital computing systems.
- Various FPGA architectures.
- Automated design flows supporting designs with FPGAs.
- Fundamentals of the FPGA design tools.
- The reconfigurable computing systems and the roles of FPGAs in those systems.

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Introduction: VLSI Design Flow, Structured Design Strategies, VLSI Design Styles, Chip Design Options. Role of FPGAs, FPGA Type, FPGA vs Custom VLSI, FPGA Based System Design. Type of ASIC, Full custom ASIC, Gate Array Based ASIC, Standard Cell Based ASIC, Different Types of Array, Design Flow, Case Study, Economics of ASIC.	(12)
2	ASIC Library Design: Transistor as Resistor, Transistor Parasitic Capacitance, Logical Effort, Predicting Delay, Logical Area, Logical paths, multistage cells, Optimum Delay, Library Cell Design, Library	(07)
3	Programmable ASICs: Anti fuse, Static RAM, EPROM & EEPROM, Practical Issues, Specification and Programmable	(05)
4	FPGA : FPGA Architectures, SRAM-Based FPGA, Permanently Programmed FPGAs, Chip I/O, Circuit Design of FPGA fabrics. ASIC I/O Cells	(05)
5	HDL : An overview of VHDL and verilog HDL, Basic concepts of hardware description languages. Structural, Data-flow and Behavioral styles, Delay modeling. Control statements, FSM modeling of hardware description. Architecture of event driven simulators.	(07)
6	Logic synthesis : Physical design compilation, simulation, and implementation. Floor planning and placement, Commercial EDA tools for synthesis.	(06)

Course Outcomes :		
1	Design and manually optimize complex combinational and sequential circuits.	
2	Model combinational and sequential digital circuits by Verilog HDL	
3	Design and model digital circuits with Verilog HDL at behavioral, structural, and RTL Levels	
4	Develop and test benches to simulate combinational and sequential circuits	
5	Be able to assess the effect of interconnect of FPGA design	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books:	Wayne Wolf, “FPGA- Based System Design” Pearson education, LPE 1st Indian Reprint.	2004
1 Reference Books	J. Bhaskar, "VHDL Primer", Pearson Education Asia	2001

2	Z. Navabi, "VHDL", McGraw Hill International Ed	1998
3	S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall NJ, USA).	1996
4	Michad John, Sebastian Smith “Application Specific Integrated Circuit”,Pearson Education, LPE	2006
5	John V. oldfield, Richard C. Dorf “Field Programmable Gate Arrays” John Wiley & Sons	1995

Course Name	:	ADVANCED VIRTUAL INSTRUMENTATION
Course Code	:	EVN 525
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
The goal is to provide students with the ability to develop a fully formed virtual instrument (VI), capable of acquiring, processing, displaying and storing real time bio-signals, by the end of the semester. Covers the basics of virtual instrumentation including use of IEEE GPIB, RS232 interfaces, and data acquisition boards. Interfacing of a computer to various instruments for data acquisition and instrument control using a state-of-the-art software platform such as National Instrument's LABVIEW.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Data Acquisition : Basic of data acquisition (Classification of signals, Real World signals, Analog Interfacing, Connecting the signal to board, Practical Vs. Ideal interfacing), Signal conditioning, DAQ Hardware Configuration, Measurement and Automation Explorer, Interfacing with assistants (DAQ assistant, analysis assistants, Instrument assistants) etc.	(07)
2	Instrument Control: Introduction, GPIB communication, Hardware specifications, Software Architecture, Instrument I/O assistant, VISA, Instrument Drivers, Serial Port Communication.	(06)
3	IMAQ Vision : Vision Basics, Image processing and analysis, particle analysis, Machine Vision, Machine Vision Hardware and Software.	(06)
4	Motion Control : Components of motion control system. Software for configuration, prototyping and development, motion controller, move types, motion amplifier and drives, feedback devices and motion I/O.	(06)
5	Virtual Instrumentation Applications (based on Lab VIEW):	(05)

	Development of a complete application in any of these fields like communication system (analog and digital communication), control system (motion control, temperature, current control etc.), Digital Signal Processing (Fourier transforms, power spectrum, correlation methods, windowing & filtering), Image acquisition and processin	

Course Outcomes :		
1	Create Virtual Instruments (VI), Edit and Debug Virtual Instruments, Build Arrays, Loops, Formulas and Sequence Structures using LabVIEW software, Customize Charts and Graphs utilizing LabVIEW software, Design a complete Data Acquisition System, Accommodate PC interfacing principles and Instrument Driver for Computer measurement and control, Employ PC ports for real time programming, Using Data Sockets to control a stepper motor over the Network	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books:	Sanjay Gupta & J.John, "Virtual Instrumentation Using LabVIEW", Electrical Engineering Series, The Tata McGraw-Hill, New Delhi, India.	2010
2	Jeffrey Travis,Jim Kring, "LabVIEW for everyone",3rd edition Pearson Education, Delhi, India.	2006
3	LabVIEW manual.	2013
1 Reference Books:	Gary Johnson, "*LabVIEW Graphical Programming*", 2nd Edition, McGraw Hill, New York.	1997
	Robert H.Bishop, "Learning with LabVIEW™ 7 Express", Pearson Education, Delhi, India.	2005
3	Lisa K. wells & Jeffrey Travis, "*LabVIEW for everyone*", Prentice Hall, New Jersey.	1997
4	Jovitha Jerome, "Virtual Instrumentation using LabVIEW",PHI Learning ,New Delhi.	2012

Course Name	:	ADVANCES IN VLSI DESIGN
Course Code	:	EVN 527
Credits	:	3
L T P	:	3 0 0

Course Objectives :

- Understand and Experience VLSI Design Flow
- Learn Transistor-Level CMOS Logic Design
- Understand VLSI Fabrication and Experience CMOS Physical Design
- Learn to Analyze Gate Function and Timing Characteristics
- Study High-Level Digital Functional Blocks
- Visualize CMOS Digital Chip Design

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Review of MOS Circuits: MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.	(04)
2	MOSFETS: MESFET and MODFET operations, quantitative description of MOSFETS: MESFET and MODFET operations, quantitative description of MOSFETS.	(05)
3	MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.	(04)
4	Short Channel Effects and Challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization	(04)
	Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode-diode logic . Defect tolerant computing.	(05)
	Super Buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General	(07)

	functional blocks - NMOS and CMOS functional blocks.	
	Special Circuit Layouts and Technology Mapping: Introduction, Talley Circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out.	(06)
	System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, Programmable structure, Gate arrays standard cell approach, Full custom design.	(07)

Course Outcomes :		
1	Understanding of a substantial body of knowledge of design methodologies and techniques applicable to VLSI technology.	
2	Design and analyze complex devices and integrated circuits using analytical tools and ability to develop new skills in these areas to a high standard.	
3	Application of knowledge together with a practical understanding of how silicon devices and others are fabricated.	
4	Advance the knowledge and understanding of current developments in VLSI technology.	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Book:	Kevin F Brnnan “Introduction to Semi Conductor Device”, Cambridge publications	2005
1 Reference Books:	Eugene D Fabricius “Introduction to VLSI Design”, McGraw-Hill International publications	1990
2	2. D.APucknell “Basic VLSI Design”, PHI Publication	2014
3	Wayne Wolf, “Modern VLSI Design” Pearson Education, Second	2002

Course Name	:	NEURAL NETWORKS
Course Code	:	EVN 529
Credits	:	3
L T P	:	3 0 0
Course Objectives :		
Understand the role of neural networks in engineering, artificial intelligence, and cognitive modeling. Provide knowledge of supervised learning in neural networks. Provide knowledge of computation and dynamical systems using neural networks. Provide knowledge of reinforcement learning using neural networks. Provide knowledge of unsupervised learning using neural networks. Provide hands-on experience in selected applications.		

Total No. of Lectures : (42)

Lecture wise Break Up		No. of Lectures
1	Introduction to artificial neural networks Biological neural networks, Pattern analysis tasks: Classification, Regression, and Clustering, Computational models of neurons, Structures of neural networks, learning principles	(04)
2	Linear models for regression and classification Polynomial curve fitting, Bayesian curve fitting, Linear basis function models, Bias-variance decomposition, Bayesian linear regression, Least squares for Classification, Logistic regression for classification, Bayesian logistic regression for classification	(08)
3	Feed forward neural networks Pattern classification using perceptron, Multilayer feed forward neural networks (MLFFNNs), Pattern classification and regression using MLFFNNs, Error back propagation learning, Fast learning methods: Conjugate gradient method, Auto associative neural networks, Bayesian neural networks	(08)
4	Radial basis function networks Regularization theory, RBF networks for function approximation, RBF networks for pattern classification	(05)
5	Kernel methods for pattern analysis Statistical learning theory, Support vector machines for pattern classification, Support vector regression for function approximation, Relevance vector machines for classification and regression	(06)
6	Self-organizing maps Pattern clustering, Topological mapping, Kohonen's self-organizing map	(05)
7	Feedback neural networks Pattern storage and retrieval, Hopfield model, Boltzmann machine, recurrent neural networks	(06)

Course Outcomes :		
1	Describe the relation between real brains and simple artificial neural network models.	
2	Explain and contrast the most common architectures and learning algorithms for Multi- Layer Perceptrons, Radial-Basis Function Networks, Committee Machines, and Kohonen Self-Organising Maps.	
3	Discuss the main factors involved in achieving good learning and generalization performance in neural network systems.	
4	Identify the main implementational issues for common neural network systems.	
5	Evaluate the practical considerations in applying neural networks to real classification and regression problems.	

Suggested Books :		
S.No.	Name of Book/ Authors/ Publishers	Year of Publication / Reprint
1 Text Books:	B.Yegnanarayana, Artificial Neural Networks, Prentice Hall of India	1999
2	Satish Kumar, Neural Networks – A Classroom Approach, Tata McGraw-Hill	2003
3	S.Haykin, Neural Networks – A Comprehensive Foundation, Prentice Hall	1998
	C.M.Bishop, Pattern Recognition and Machine Learning, Springer	2006

Course Name	:	LAB I Based on VHDL and Cadence Tool
Course Code	:	EVN 518
Credits	:	2
L T P	:	0 0 3
Course Objectives :		
The objective of this lab is to familiarize the students with the basics of the Cadence® Custom IC design tool, Virtuoso®. You will first set up your account to run the IC tool, learn how to manage your files with the Library Manager, understand the basics of the Schematics Editor, and simulate a simple circuit using the Analog Design Environment (ADE). Understand the differences between using ideal and real circuit elements. Cadence Education Learning Maps provide a comprehensive visual overview of the learning opportunities for Cadence customers, helping you navigate our curriculum of offerings based on your level of competency.		

Total No. of turns : (14)

List of Experiments		No. of Turns
	Write VHDL code for the following 1. LOGIC EXPRESSIONS 2. MODULO SYNCHRONOUS UP-DOWN COUNTER 3. MULTIPLERXERS/DECODERS 4. DESIGN OF ALU 5. PRIORITY ENCODER 6. 4-BIT MAGNITUDE COMPARATOR 7. PARITY GENERATOR 8. LINEAR CONVOLUTION 9. CIRCULAR CONVOLUTION 10. AUTO-CORRELATION 11. CROSS-CORRELATION 12. FFT USING DIF 13. IFFT USING DIF 14. FFT USING DIT 15. IFFT USING DIT 16. DESIGN OF BUTTER WORTH FILTER USING IMPUSE INVARIANT METHOD 18 DESIGN OF LPF USING HAMMING WINDOWS 19. DFT 20. MOORE MODEL 21. MEALY MODEL CADENCE BASED EXPERIMENTS : 1. DESIGN THE MOS TRANSISTOR CIRCUITS FOR DC & AC SMALL SIGNAL PARAMETERS, COMPLETING THE DESIGN FLOW MENTIONED BELOW: A. DRAW THE SCHEMATIC AND VERIFY THE FOLLOWING I) DC ANALYSIS II) AC ANALYSIS III) TRANSIENT ANALYSIS B. DRAW THE LAYOUT AND VERIFY THE DRC, ERC C. CHECK FOR LVS. 2. DESIGN A SIMPLE SAMPLE AND HOLD CIRCUIT AND MEASURE THE SWITCHING TIMES. 3. DESIGN A PLL AND MEASURE ALL THE PARAMETERS.	02 02 02 02 02 01 01 02

	4. DESIGN A SIMPLE ADC/DAC AND MEASURE THE DATA CONVERSION TIME. ASSUME THE 95 NANOMETER TECHNOLOGY. 5. DESIGN 3-8 DECODER USING MOS TECHNOLOGY	

Course Outcomes :		
1	Students are able to use Cadence Virtuoso Platform for verification of functionality and simulation of RTL Verilog model. Generally Virtuoso Platform used for designing full-custom integrated circuits includes schematic entry, behavioral modeling (Verilog-AMS), circuit simulation, full custom layout, physical verification, extraction and back-annotation.	

Course Name	:	LAB II Based on ARM Processor and INTEL ATOM Processor
Course Code	:	EVN 528
Credits	:	2
L T P	:	0 0 3
Course Objectives :		
The objective of this lab is that the students can learn the ARM and Intel ATOM processor. Learn the internal architecture of these processors, differentiate between these processors and also learn the functionality of these processors. Application of ARM and Intel ATOM processors.		

Total No. of Labs : (14)

List of Experiments		No. of Turns
1	List of experiments 1. Familiarization with ARM processor kit 2. Addition of two 16-bit numbers 3. Dissemble a byte into higher and lower nibble 4. Addition of two 64-bit numbers 5. Look up the factorial of a number from the table by using address of the memory location 6. Add a series of 16-bit numbers using table address 7. Scan a series of 16-bit numbers and find how many are negative 8. Multiply two 16-bit binary numbers. 9. Divide a 32-bit number by a 16-bit number and store the quotient and remainder 10. Convert a single hex digit into its ASCII equivalent. 11. Add two packed BCD numbers and store the result. 12. Write a subroutine to find a factorial of a number (the number is	1 per week

	passed from the main program) 13. Familiarization with INTEL ATOM kit 14. Applications based on INTEL ATOM kit	

Course Outcomes :		
1	The benefits of these approaches are to reduce cost, heat, and power usage compared to more complex chip designs, traits which are desirable for light, portable, battery-powered devices such as smart phones and tablet computers. The students are able to implement and compare the logic using two processors.	