Curriculum M.Tech VLSI Design
2022-23 Batch Onwards

VISION Of the Department:

The Department aims to be recognized as centre of excellence in Electronics and Communication Engineering by continuously striving to achieve excellence in providing Education, Research, and Innovation**.**

MISSION Of the Department:

1. To provide our graduates with state of art facilities, experienced engineering education that balances both theoretical and practical knowledge for the design, analysis and operation of electronic systems in order to meet the needs of the relevant industry and research organization.

2. To conduct research in the field of Electronics and Communication Engineering focusing in the emerging research areas such as advanced communication systems, VLSI, Photonics systems, embedded systems etc.
3. To promote the overall development of graduates by encouraging them to participate in co-curricular and extra-curricular activities & providing awareness of ethical values in order to prepare them to face the challenges of the changing world.
4. To build relationship with Alumni to create a network and support for the department.
5. To design the curriculum through a continuous process in consultation with stakeholders so that the students graduating from the department have top rating in placement.

PEOs, POs, and PSOs
M.Tech (VLSI Design)

Programme Educational Objectives

This programme prepares graduates to

1. Be technically competent in design, development and implementation of electronics and VLSI design and extends into applications in the different thrust areas.

2. Possess suitable knowledge for analysing, modelling, and evaluating the research problems in major thrust areas of VLSI design.

3. Possess interpersonal skills, team work capabilities, communication skills, leadership and awareness of the social, ethical and legal responsibilities leading to lifelong learning and career development.

4. Be successfully employed in electronics profession in industry/ research organization and to have entrepreneurial skill.

Program Outcomes (POs):

PO1: An ability to independently carry out research /investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

Programme Specific Outcome (M.Tech (VLSI DESIGN))

PSO 01

Ability to attain, identify and apply knowledge of mathematics, science & engineering in Electronics VLSI design discipline to the solution of various engineering problems.

PSO 02

Ability to develop the design capability among students so that they have the ability to participate in creative, synthetic and integrative activities of the relevant branch of engineering.

PSO 03

Ability to use techniques and modern CAD Tools so as to implement them in engineering practice to develop professional skills that will prepare the students for immediate employment in the relevant branch of engineering in industry.

Semester wise PG Scheme for M.Tech. Programme (VLSI Design) w.e.f. 2022-23 session

Semester I

Sr. No.	Course Stream	Course Name - Course Code	Credits	L-T-P
1.	Program Core Course	Electronic System Design **(EVR1101)**	3	2-0-2
2.	Program Core Course	Digital VLSI Design **(EVR1102)**	3	2-0-2
3.	Program Core Course	Solid State Devices **(EVR1103)**	3	3-0-0
4.	Deptt. Elective Course (DEC-I)	• Low Power Sub-System Design & Technology **(EVR1201)** • Semiconductor Memory Design & Testing **(EVR1202)** • FPGA Based System Design **(EVR1203))** • Mixed Signal IC Design **(EVR1204)**	3	2-0-2 2-0-2 2-0-2 3-0-0
5.	Design of experiments and research methodology	Design of experiments and research methodology **(EVR 1001)**	3	2-0-2
6.	Soft Computing /Soft Skills & Management	Soft Computing /Soft Skills and Management **(SMR1001)**	3	
		Total Credits	**18**	

Semester II

Sr. No.	Course Stream	Course Name - Course Code	Credits	L-T-P
1.	Program Core Course	Computer Aided VLSI Design **(EVR1104)**	3	2-0-2
2.	Program Core Course	Testing & Fault Tolerance **(EVR1105)**	3	3-0-0
3.	Program Core Course	Analog CMOS Design **(EVR1106)**	3	2-0-2
4.	Deptt. Elective Course (DEC-II)	• Real Time Embedded System **(EVR1251)** • VLSI Technology **(EVR1252)** • Semi-Conductor Devices Modelling **(EVR1253)** • Optoelectronic materials and devices **(EVR1254)**	3	2-0-2 3-0-0 3-0-0 3-0-0
5.	Open Elective	• Neural Networks **(EVR3001)** • Flexible Electronic materials and circuits **(EVR3002)** • Neuromorphic Engineering **(EVR3003)** • Sensors & Actuators **(EVR3004)**	3	3-0-0 3-0-0 3-0-0 3-0-0
6.	Engineering Mathematics		3	
7.	Industrial Tour	**EVR4001**		
		Total Credits	**18**	

Semester III

Sr. No.	Course Name /Course Code	Credits
1.	Seminar and Report Writing **(EVR5001)**	2
2.	Research and Publication Ethics **(RPR6001)**	2
3.	Dissertation-I **(EVR7001)**	14
	Total	**18**

Semester IV

Sr. No.	Course Name /Course Code	Credits
1.	Dissertation-II **(EVR8001)**	18
	Total	**18**

Semester 1
Core

Course Name	**:**	**ELECTRONIC SYSTEM DESIGN**
Course Code	**:**	**EVR 1101**
Credits	**:**	**3**
L T P	**:**	**2-0-2**

Total No. of Lectures: 28

Total No. of Lab Hours: 28

Course Objectives:

The main objectives of this course are:

1. To introduce the students to the fundamental of Hardware Description Language.
2. To introduce the student to the fundamentals of combinationaland sequential(both synchronous and asynchronous) logic design.
3. To develop an understanding of optimized circuits design and analyze them using various techniques
4. To get acquainted with the concepts of digital system design.

Course Contents

S.No.	Lecture wise breakup	No. of lectures
1	**Design Concepts and Logic Circuits** Digital Hardware, Design Process, Design of Digital Hardware, Basic concepts of Hardware description languages, An overview of VHDL programming: Structural, Data-flow and Behavioural styles, Delay modelling, Control statements, FSM modelling of hardware description language, Datatypes, Operators, Concurrent and Sequential Code, Signal and Variable, Package.	10
2	**Optimized Implementation of Combinational Logic Circuits** Strategy for minimization, Incompletely specified functions, Multiple output circuits, Multilevel synthesis & Analysis. Building Blocks: Multiplexers, Decoders, Encoders Code Converters and their implementation in VHDL, Programmable Logic Devices: PROM, PLA, PAL, FPGA and CPLDs.	6
3	**Synchronous and Asynchronous Sequential Circuits** Synchronous sequential circuits, basic design steps, Mealy state model, Design of FSM and their implementation using VHDL programming. Asynchronous sequential circuits analysis, synthesis, state reduction, state assignment, hazards.	7
4	**Digital System Design** Digital system design, building block circuits, Algorithm state machines: ASM Charts, Pseudo codes, Data-path and control path circuits(Bit counting circuit, Divider, Shift and Add Multiplier etc.), Static timing Analysis, Clock Skew and Clock latency.	5

Lab Work

Sr. No	Lab Module	No. of Hours 28
1	Simulation and synthesis of Digital circuits with VHDL using Xilinx ISE: a) Test vector generation and timing analysis of sequential and combinational logic design realized using VHDL. b) Verification of the functionality of designed circuits using function simulator.	7 7
2	Write a test bench to verify the correctness of the designed Digital VLSI circuits: Up-front verification becomes very important as designed circuits increases in size and complexity.	14

Course outcomes:

At the completion of this course, students will be able to:	
1	Evaluate and create the PLD based designs using both schematic capture and VHDL
2	Able to perform simulation and synthesis of various combinational and sequential circuits using VHDL
3	Design, build and debug optimized complex combinational circuits
4	Analyze the combinational and sequential circuits based on an abstract functional specification using VHDL.
5	Establish comprehensive understanding of the digital system design

Bibliography:

Sr. No.	Book Detail	Year of Publication
1.	Alan B. Marcovitz," Introduction to Logic Design", Third Edition, McGraw Hill.	2010
2.	Ronald J. Tocci, Neal S. Widmer& Greg Moss, Digital Systems, Global Edition, 12/E,Pearson Education Limited.	2016
3.	Bhaskar, A VHDL Primer, Third Edition, Prentice Hall.	2017
4.	Morris Mano, M. ,Digital Logic and Computer Design, Pearson Education Limited.	2016
5.	Research and review papers in specific area.	

	PO1	PO2	PO3
CO1	2	2	3
CO2	2	2	3
CO3	2	2	3
CO4	2	2	3
CO5	1	1	3

Course Name	**:**	**Digital VLSI Design**
Course Code	**:**	**EVR 1102**
Credits	**:**	**3**
L T P	**:**	**2-0-2**

Total No. of Lectures: 28
Total No. of Lab hrs. : 28

Course Objectives:

1. To introduce the students to the fundamental principles of VLSI circuit design
2. To examine the basic building blocks of large-scale digital integrated circuits.
3. To introduce the students the modeling of the various semiconductor devices for digital VLSI circuit design.
4. To comprehend static and dynamic CMOS logic circuits.

Course Contents:

Sr. No	Course Contents	No. of Lectures
1.	**Circuit Characterization and Performance Estimation:** Delay Estimation, RC delay models, Linear delay Models, logical effort, parasitic delay. Logical effort and transistor sizing: Delay in logic gate, Delay in Multistage logic network, static and dynamic power dissipation.	**8**
2.	**Interconnects:** Interconnect parameters: resistance and capacitance., distributed RC delay, L-Model, π-Model, T-Model approximations. Crosstalk, crosstalk delay effects, crosstalk noise effects.	**4**
3.	**Combinational logic:** Static CMOS Design, Synthesis of complex CMOS Gates, Ratioed Logic, Pass Transistor Logic, various logic circuits using pass transistors. Dynamic CMOS Design: Dynamic Logic, basic principles, charge leakage and sharing in Dynamic Logic, capacitive coupling, clock feedthrough.	**8**
4.	**Sequential logic**: Static latches and flip-flops (FFs), dynamic latches and FFs, Clock strategies for sequential design, sense-amplifier based FFs, NORA-CMOS logic, Schmitt trigger, monostable and astable circuits.	**8**

SNo.	List of Experiments:	Total lab Hr. 28
1.	Capture the schematic of CMOS inverter and compute the following from simulation resuls: a. tp_{HL}, tp_{LH} and t_d . b. Tabulate the delay and find the best geometry for minimum delay for CMOS inverter?	4
2	Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.	6
3	Capture the schematic of 2-input CMOS NAND gate having best geometry of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay t_d for all four possible combinations of input vectors. Tabulate the results. Then increase the drive strength to 2X	4

	and 4X and tabulate the observations.	
4	Draw layout of 2-input NOR with Wp/Wn = 40/20, use optimum layout methods. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Tabulate the results. Then increase the drive strength to 2X and 4X and tabulate the observations.	6
5	Individual projects have to be carried out for this course.	8

Course Outcomes:

At the completion of this course, student will be able to:	
1	Design logic circuit layouts for both static CMOS and dynamic clocked CMOS circuits.
2	Compute and estimate the power consumption of a VLSI chip.
3	Analyze VLSI circuit timing using logical effort analysis.
4	Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits.
5	Analyze the effect of interconnect parameters on crosstalk delay and noise.

Bibliography:

Sr. No	Book Detail	Year Publication
1	Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design,: A Circuits and Systems Perspective, 3rd edition.	2008
2	Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits – A Design Perspective, Pearson Education 2nd edition.	2007
3	Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill 3rd edition	2008
4	Baker, R.J, CMOS Circuit Design, Layout and Simulation, Wiley – IEEE Press, 2nd edition	2010
5	Research and review papers in specific area.	

	PO1	**PO2**	**PO3**
CO1	2	1	3
CO2	3	1	2
CO3	3	1	3
CO4	3	2	3
CO5	2	1	3

Course Name	**:**	**SOLID STATE DEVICES**
Course Code	**:**	**EVR1103**
Credits	**:**	**3**
L T P	**:**	**3-0-0**

Course Objectives:

By the end of this course, the students will be able to:

1. Explain the semiconductor device physics
2. Understand formation of p-n junctions, p-n junction devices, fabrication, electrical characteristic
3. Provide detailed analysis off MOSFET and its various versions.
4. Understand Moore's Law, scaling of MOSFET and its impact in revolutionizing the electronic market including high speed processors and consumer electronic products.

Total No. of Lectures: 42

	Lecture wise breakup	**No. of Lectures**
1.	MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, LFCV and HFCV, Nonidealities in MOS, oxide fixed charges, interfacial charges, Midgap gate Electrode, Poly-Silicon contact, Electrostatics of non-uniform substrate doping, ultrathin gate-oxide and inversion layer quantization, quantum capacitance, MOS parameter extraction	(10)
2.	Physics of MOSFET: Drift-Diffusion Approach for IV, Gradual Channel Approximation, Sub-threshold current and slope, Body effect, Pao & Sah Model, Detail 2D effects in MOSFET, High field and doping dependent mobility models, High field effects and MOSFET reliability issues (SILC, TDDB, & NBTI), Leakage mechanisms in thin gate oxide, High-K-Metal Gate MOSFET devices and technology issues, Intrinsic MOSFET capacitances and resistances, Meyer model	(8)
3.	SOI MOSFET: FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, VT definitions, Back gate coupling and body effect parameter, IV characteristics of FDSOI-FET, FDSOI-sub-threshold slope,Floating body effect, single transistor latch, ZRAM device, Bulk and SOI FET: discussions referring to the ITRS	(8)
4.	Nanoscale Transistors: Diffusive, Quasi Ballistic & Ballistic Transports, Ballistic planer and nanowire-FET modeling: semi-classical and quantum treatments	(5)
5.	Advanced MOSFETs :Strain Engineered Channel materials, Mobility in strained materials, Electrostatics of double gate, and Fin-FET devices	(6)
6	High Electron Mobility Transistor (HEMT): physical structure of HEMT, quantum well structures, 2D electron gas density, chargevoltage relation, current voltage characteristics, cut-off frequency	(5)

Course Outcomes: By the end of this course, the students will be able to	
1.	Explain the physics of various solid state devices such as MOSFETS, SOI devices and other advanced nano electronic devices.

2.	Understand the importance of electrons and holes in semiconductors, the charge density and distribution, the charge transport mechanisms.
3.	Understand the concept of modelling advanced nano transistors and the use of novel materials for the design of FinFET devices.
4.	Justify the development of FinFET and nanoscale transistors due to MOSFET reliability issues with latest technology nodes
5.	Understand the characteristics of advanced compound semiconductor transistors for high speed electronics.

Suggested Books:

Sr. No.	Name of Book/Authors/Publisher	Year of Publication /Reprint
1	S.M. Sze & Kwok K. Ng, Physics of Semiconductor Devices, Wiley 2007 n 23.	**Latest Edition**
2	K. Hess, Advanced Theory of Semiconductor Devices, Prentice-Hall, 1988.	**Latest Edition**
3	. Yuan Taur & Tak H. Ning, Fundamentals of Modern VLSI Devices, Cambridge 1998	**Latest Edition**
4	Mark Lundstrom & Jing Guo, Nanoscale Transistors: Device Physics, Modelling & Simulation, Springer 2005	**2005**
5	Yannis Tsividis, Operation and Modelling of the MOS Transistor, Oxford University Press 2 nd Edn.	**Latest Edition**
6	J.P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Springer 1997	**Latest Edition**
7	Singh, Semiconductor Devices: Basic Principles, Wiley, 2000	**2000**
8	Michael Shur, Physics of Semiconductor Devices, Prentice Hall, first published in 1990	**Latest Edition**

CO	PO1	PO2	PO3
CO1	**-**	**-**	**2**
CO2	**-**	**-**	**2**
CO3	**1**	**-**	**2**
CO4	**2**	**3**	**3**
CO5	**2**	**2**	**3**

Course Name	**:**	**Design of Experiments and Research Methodologies**
Course Code	**:**	**EVR1001**
Credits	**:**	**3**
L T P	**:**	**2 0 2**
Segment	**:**	**1-6**

Total No. Lectures: 28

Total No. of Lab hrs. 28

Course Objectives:

The main objectives of this course are:

- To develop an understanding of how to identify research topics, formulate research questions / hypotheses, select an appropriate research and, where applicable, experimental design.
- To provide a basis so the student can effectively develop a research proposal for either a capstone project, master's thesis, research project, or designed experiment.

Course Contents:

Module-I (Common for all branches)

Sr. No.	**Course contents**	**No. of Lectures**
1.	Introduction: Types of Research and Their Purposes, Locating, Analysing, stating and evaluating research problem, need for literature review, steps in conducting literature review, SWOT analysis, research questions and hypothesis, types of hypothesis, evaluation of hypothesis.	**4**
2.	Data Collection and Analysis: Accepts of method validation, observation and collection of data, methods of data collection, sampling methods, data processing and analysis strategies and tools, data analysis with statically using available tool and package , hypothesis testing.	**6**
3.	Procedure for writing a research report and manuscript: Types of research reports, steps of writing a report, layout of report, layout of research paper, ethical issues related to publishing, Plagiarism and Self-Plagiarism.	**4**
4	Research Design and Sampling Design: Concept of research design, features of a good research design, concept of population and sample, characteristics of sample design, types of sampling techniques	**6**
5	Ethics-ethical issues, ethical committees (human & animal); IPR- intellectual property rights and patent law, commercialization, copy right, royalty, trade related aspects of intellectual property rights (TRIPS); scholarly publishing-IMRAD concept and design of research paper, citation and acknowledgement, plagiarism, reproducibility and accountability	**8**

Lab Work:

Sr. No.	Lab contents	No. of Hours
1.	Select a problem from your area of interest, identifying the type of research problem it is and perform the SWOT analysis of the existing literature.	4
2.	Generate research questions and hypotheses for a problem from your area of interest.	4
3.	Design a questionnaire for the problem of interest.	4
4.	Interpretation of Data and Paper Writing – Layout of a Research Paper, Finding journal, Ethical issues related to publishing, Plagiarism and Self-Plagiarism.	4
5.	Use of tools / techniques for Research: methods to search required information effectively, Reference Management Software like Zotero/Mendeley, Software for paper formatting like LaTeX/MS Office.	6
6.	Preparing a research paper for the problem of interest	6

Course Outcomes:

At the completion of this course, students will be able to:	
1.	Developed an understanding of how to identify research topics, formulate research questions and corresponding hypotheses, select an appropriate research and where applicable, experimental design.
2.	Perform required statistical analyses for any univariate application in a business / industrial setting, regardless of data form, and will be familiar with major indices for measuring correlation and association.
3.	Further, the underlying assumptions related to each statistical test and its interpretation will be thoroughly reviewed.

Bibliography:

Sr. No.	Book Detail	Year of Publication
1.	Probability and Statistics for Engineers and scientists by Anthony J. Hayter, Cencage Learning, 4th Edition	2016
2.	Probability and Statistics for Engineers and scientists by Walpole, Myers, Myers and Ye, 8th ed Pearson Education	2007
3.	Research Methodology - Methods and Techniques, C. K. Kothari, New Age International, 2nd Edition	2004
4.	English for writing research papers by Adrian Wallwork, 2nd Edition. Springer	2016
5.	Statistics: Concepts and Controversies by David S. Moore, William I. Notz, W. H. Freeman	2016

CO-PO Mapping:

CO	PO1	PO2	PO3
CO 1	1	3	-
CO2	1	3	-
CO3	-	3	-
CO4	-	3	-
CO5	-	3	-

DEC 1

Course Name	:	**Low Power Subsystem Design and Techniques**
Course Code	**:**	**EVR1201**
Credits	**:**	**3**
L T P	**:**	**2 0 2**
Segment	**:**	**1-6**

Total No. of Lectures: 28

Total No. of Lab Hours: 28

Course Objectives:

The main objectives of this course are:

1. To introduce the students to the state-of-the-art techniques for optimization of systems. Power is the vital design constraint in almost all electronic devices, battery operated applications. For low power design of digital systems.
2. To introduce the students to the the methods and tools for power optimization used at all stages of the design development flow (i.e., from system specification to implementation).
3. To introduce the students to the usage of the some of the industry standard tools for low power design through Lab sessions.
4. To introduce the students to an exhaustive review of methods for power estimation of digital VLSI subsystems.
5. To introduce the students to the usage of industry standard tool for lowpower design through Lab sessions.

Sr. No	Course Contents	No. of Lectures
1.	**Need for Low Power VLSI Chips:** Introduction, sources of power dissipation in digital Integrated circuits. Emerging low power approaches, estimation of power dissipation due to switching, short circuit, sub-threshold leakage, and diode leakage currents. Device & technology impact on low power, dynamic dissipation in CMOS. Impact of technology, scaling , transistor sizing and gate oxide thickness on power dissipation	**8**
2.	**Power Analysis and Optimizations :** Threshold voltage scaling and control, multiple threshold CMOS (MTCMOS), Substrate bias controlled variable threshold CMOS, testing issues: Design and test of low-voltage CMOS circuits. Circuit and logic style, adiabatic logic circuits. Power analysis and optimization, Power analysis techniques, energy recovery techniques, software power estimation and optimization of lowpower memory circuits and architectures	**7**

3	**Low power Architecture & Systems Power:** Low power Architecture, systems power and performance management, switching activity reduction, parallel architecture with voltage reduction, low power arithmetic components, low power low voltage adder design approaches, multiplier design approaches and low power memory design, Low-Power Memory Circuits and architectures.	**6**
4	**Low Power Clock Distribution And Special Techniques**: Power dissipation in clock distribution, single driver vs distributed buffers, zero skew vs tolerable skew, chip and package co design of clock network. Power reduction in clock networks, CMOS floating node, low power bus delay balancing, and low power techniques for SRAM. Power conscious high level synthesis, silicon on insulator based technologies.	**7**

Lab Work

Sr No.	**Device Modelling and Simulation**	No. of Hours 28
1.	Introduction to CADENCE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis). Design the circuits and verify the following: i) DC Analysis ii) AC Analysis iii) Transient Analysis.	6
2.	To identify the problem statement, analyze and compare the various parameters.	4
3.	Introduction to CADENCE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis) Design adder and subtractorcircuit usinguniversal gates and verify its output. Design a full adder using half adder.Design a latch specifying some time constraints using universal gates. Design decoder using MOS technology.	10
4.	To identify the problem statement, analyze and compare the various parameters.	4
5.	Projects and case study with the latest tools available in the respective lab.	4

Course Outcomes

At the successful completion of this course, student will be able to:	
1.	Use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnect.
2.	Create models of moderately sized CMOS circuits that realize specified digital functions
3.	Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect, and to verify the functionality, timing, power, and parasitic effects.
4.	Design chips used for battery-operated systems and high-performance circuits not exceeding power limits..
5.	Understand the concepts of low voltage, low power logic circuits
6.	Recognize advanced issues in VLSI systems, specific to the deep-submicron silicon

	technologies.

Bibliography:

Sr.No	Book Detail	Year of Publication
1.	Roy, K. and Prasad, Sharat C., Low Power CMOS VLSI: Circuit Design, John Wiley.	2000
2.	Kiat-Seng Yeo, Roy K., Low voltage Low power VLSI subsystems, Tata Mcgraw-Hill	2004
3.	Rabaey,J,M. and Pedram, M., Low power design methodologies,Springer.	1996
4.	Chandrakasan, A.P. and Broderson, R.W., Low Power Digital CMOS Design, Kluwer	1995
5.	Research and review papers in specific area.	

	PO1	**PO2**	**PO3**
CO1	3	1	3
CO2	3	1	3
CO3	3	1	2
CO4	3	1	3
CO5	3	1	2
CO6	3	1	3

Course Name	:	**Semiconductor Memory Design and Testing**
Course Code	**:**	**EVR1202**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Total No. of Lectures: 28

Total No. of Lab Hours: 28

Course Objectives:

The main objectives of this course are:

1. To learn about SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies.
2. To learn about different memory devices like RAM, ROM, PROM, EPROM, EEPROM, etc.
3. To get acquainted with different terms like read, write, access time, nibble, byte, bus, word length, address, volatile, non-volatile, etc. How to implement combinational and sequential circuit using ROM.
4. To learn RAM fault modeling and testing for memory.
5. To learn about Ferroelectric RAMs (FRAMs), analog memories, magneto resistive RAMs (MRAMs), MCM (3D and 2D),hybrid memory, MCM testing and reliability issues, memory cards, high density memory packaging future directions.

Sr. No	Course Contents	No. of Lectures
1.	**STATIC RANDOM ACCESS MEMORY(SRAM) TECHNOLOGIES:** SRAM cell structure, MOS SRAM, Architecture-MOS SRAM cell and peripheral circuit operation, bipolar SRAM technologies-silicon on insulator (SOI) technology, advanced SRAM architectures and application specific SRAMs.	**5**
2.	**DRAM TECHNOLOGIES AND NON-VOLATILE MEMORIES:** DRAM technology development CMOS , DRAM-DRAM cell theory and advanced cell structures, BiCMOS, DRAMs-soft error failures in DRAMs-Advanced DRAM designs and architecture-application, Specific DRAMs. Masked read-only memories (ROMs)-High density ROMs-programmable read-only memories (PROMs)- bipolar PROMs-CMOS PROMs-Erasable (UV) – Programmable road-only memories (EPROMs)-floating-gate EPROM cell-one- time programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM technology and architecture, nonvolatile SRAM-flash memories (EPROMs or EEPROM), advanced flash memory architecture.	**6**

3.	**SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS:** General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability, Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques	**5**
4.	**MEMORY FAULT MODELLING:** RAM fault modeling, electrical testing, pseudo random testing-megabit DRAM testing, non-volatile memory modeling and testing-IDDQ fault modeling and testing-application specific memory testing, memory-subsystem technologies, high-performance standard DRAMS, embedded memories.	**7**
5.	**ADVANCED MEMORY TECHNOLOGIES AND HIGH-DENSITY MEMORY PACKING TECHNOLOGIES:** Low-power memory circuits: sources and reduction of power dissipation in a ram subsystem and chip, low-power dram circuits, low power SRAM circuits. Content Addressable Memories (CAMs) Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory stacks and MCMs (3D), Memory MCM testing and reliability issues, memory cards, high density memory packaging future directions.	**5**

Lab Work

Sr No.	**Device Modelling and Simulation**	No. of Hours 28
1.	Introduction to CADENCE (Operating Point Analysis, Transient Analysis, Parametric Sweep). Design SRAM cell and calculate it's delay parameter. Comparison of SRAM cell using 180nm and 90nm technology.	6
2.	To identify the problem statement, analyze and compare the various SRAM cell.	4
3.	Introduction to CADENCE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis. Design memory with write and read operation.	6
4.	To identify the problem statement, analyze the various memory related issues.	6
5.	Projects and case study with the latest tools available in the respective lab.	6

Course Outcomes

At the successful completion of this course, student will be able to:	
1.	Describe the technology used in the construction of digital memory and assess the quality of various memory types.

2.	Draw the schematic of a static and dynamic memory cell and explain in details the process of reading and writing a bit of information in it.
3.	Learn about SRAM – SRAM Cell structures, MOS SRAM architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, advanced SRAM architectures and technologies.
4.	Able to learn RAM fault modelling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modelling and testing.
5.	Able to learn IDDQ fault modelling and testing, Application specific memory testing,RAM fault modelling, BIST techniques for memory
6.	Able to learn about Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D)

Bibliography:

Sr.No	Book Detail	Year of Publication
1.	Ashok K.Sharma," Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of India Private Limited, New Delhi.	2007
2.	Tegze P .Haraszti, "CMOS Memory Circuits", Kluwer Academic Publishers.	2003
3.	Betty Prince, "Emerging Memories: Technologies and Trends", Kluwer Academic publishers.	2002
4.	Research and review papers in specific area.	

	PO1	PO2	PO3
CO1	3	1	3
CO2	3	1	2
CO3	3	1	2
CO4	3	1	3
CO5	3	1	2
CO6	3	1	3

Course Name	**FPGA Based System Design**
Course Code	**EVR1203**
Credits	**3**
L T P	**2 0 2**

Total No. Lectures: 28
Total No. of Lab hrs. 28

Course Objectives:

The main objectives of this course are:

1. To understand automated design flow for designs with FPGAs.
2. To understand concepts, architecture and embedded components of .
3. To understand different technologies to configure FPGA.
4. To explore the development and deployment of FPGA based digital systems

Course Contents:

Sr. No.	Course contents	No. of Lectures
1	**Fundamentals concepts of FPGA** VLSI Design Flow, Design Hierarchy, VLSI Design Styles, Types of ASIC, Full custom ASIC, Gate Array Based ASIC, Standard Cell Based ASIC, FPGA versus ASIC.	3
2	**Review of HDL** Basic concepts of hardware description languages, An overview of Verilog HDL, Gate level, Data-flow, Behavioral and switch level modeling, task and functions. Timing and delays, User defined primitives.	8
3	**FPGA architectures:** Fuse, Antifuse, PROM, EPROM, EEPROM, Flash and SRAM based FPGAs, Xilinx CPLD Architecture, Circuit Design of FPGA fabrics. Fine, medium and coarse-grained architectures. MUX and LUT-based logic blocks, Fast carry chain.	3
4	**Programming (Configuring) an FPGA:** Configuration files, configuration cells, programming using configuration port, JTAG in brief, programming using JTAG port.	4
5	**Embedded blocks in FPGA and Logic Synthesis:** Embedded RAMs, Embedded multipliers, adders, MACs, Embedded processor cores (hard and soft), Clock trees and clock managers, General- purpose I/O, Gigabit transceivers, Hard IP, Soft IP and Firm IP, System gates versus real gates. Commercial EDA tools for synthesis, advanced FPGA applications.	6
6	**Case study:** Xilinx Virtex (Architecture) FPGA, Kintex-7/Zynq-7000	4

Lab contents	No. of Hours 28
1. Simulation, implementation and synthesis of digital circuits using Verilog in Xilinx ISE simulator of sequential and combinational logic like various Flipflops, address decoder, Tristate buffer, Multiplexer etc. concurrent code and using sequential code. 2. Synthesis of digital circuits will be carried out on FPGA kits. 3. Design and analysis based Project for various digital systems using FPGA kits.	10 8 10

Course Outcomes:

At the completion of this course, the students will be able to:	
1.	Understand the design model, method, criterion and steps of FPGA design.
2.	Understanding the configuration of FPGA.
3.	Learning the performance specification of FPGA devices.
4.	Design and model digital circuits with HDL at behavioral, structural, and RTL Levels.
5.	Develop and test benches to simulate combinational and sequential circuits.

Bibliography:

Sr. No.	Book Detail	Year of Publication
1	Wayne Wolf, FPGA - Based System Design, Pearson education, LPE 1st Indian Reprint	2004
2	Michad John, Sebastian Smith, Application Specific Integrated Circuit, Pearson Education	2006
3	John V. Oldfield, Richard C. Dorf, Field Programmable Gate Arrays, John Wiley & Son	1995
4	Maxfield, Clive. The design warrior's guide to FPGAs: devices, tools and flows. Elsevier	2004
5	Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall PTR 2nd Ed	2003
6	Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, 2nd edition	2011
7	Research and Review papers in specific area	

	PO1	PO2	PO3
CO1	1	3	2
CO2	1	2	2
CO3	3	2	2
CO4	3	2	3
CO5	3	1	3

Course Name	:	**MIXED SIGNAL IC DESIGN**
Course Code	**:**	**EVR1204**
Credits	**:**	**3**
L T P	**:**	**3-0-0**

Total No. Lectures: 42

Course Objectives:

The main objectives of this course are:

1. To teach advance design techniques for bandgap references, comparators, ADC/DAC, oscillators and PLL.
2. To design the product level design blocks for VLSI applications.

Course Contents:

Sr.No	Course Contents	No. of Lectures
1.	**Sample and hold and trans-linear circuits** Performance of sample-and-hold circuits – testing sample and holds, MOS sample-and-hold basics, examples of CMOS S/H Circuits, bipolar and BiCMOS Sample-and-Holds, Bandgap Voltage Reference, Circuits for Bandgap Reference	**7**
2.	**Switched Capacitor circuits** Basic building blocks – opamps, capacitors, switches, non-overlapping clocks, Basic operation and analysis of switched capacitor circuits, resistor equivalence of a switched capacitor, parasitic-sensitive integrator, parasitic-insensitive integrators, signal-flow-graph analysis, noise in switched-capacitor circuits.	**7**
3.	**Comparators** Comparator specifications – input offset and noise, hysteresis, Opamp as a comparator – input-offset voltage errors, charge-injection errors, making charge-injection signal independent, minimizing errors due to charge-injection, speed of multi-stage comparators, Latched comparators, latch-mode time constant, latch offset, examples of CMOS and BiCMOS comparators, input-transistor charge trapping	**7**
4.	**Data Converter Architectures** DAC Architectures- Resistor string, R-2R ladder Networks, Current Steering, Charge Scaling DACs, Cyclic DAC, and Pipeline DAC. ADC Architectures- Flash, Two-step flash ADC, Pipeline ADC, Integrating ADC's, Successive Approximation ADC.	**7**
5.	**Data Converter Modeling And SNR** Sampling and Aliasing: A modeling approach, Impulse sampling, The sample and Hold, Quantization noise. Data converter SNR: An overview, Clock Jitter, Improving SNR using Averaging, Decimating filter for ADCs, Interpolating filter for DACs, Band pass and High pass sinc filters - Using feedback to improve SNR.	**8**
6.	**OSCILLATORS AND PLL** LC oscillators, Voltage Controlled Oscillators. Simple PLL, Charge pumps PLLs, Non ideal effects in PLLs, Delay Locked Loops.	**6**

Projects and case study with the latest tools available in the respective lab.

Course Outcomes

At the completion of this course, students will be able to:	
1	Apply the concepts for mixed signal MOS circuit.

2	Analyze the characteristics of IC based CMOS amplifiers.
3.	Design of various data converter architecture circuits.
4.	Analyze the signal to noise ratio and modeling of mixed signals.
5.	Design of oscillators and phase lock loop circuit

Bibliography:

Sr.No	Book Details	Year of Publication
1	Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill	2008
2	Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press, 2nd Edition	2002
3	Johns, D.A. and Martin, K., Analog Integrated Circuit Design, John Wiley	2008
4	R. Jacob Baker, CMOS Mixed Signal Circuit Design, Wiley India	2008
5	Research and review papers in specific area	

	PO1	**PO2**	**PO3**
CO1	3	1	3
CO2	3	1	3
CO3	3	1	2
CO4	3	1	2
CO5	3	1	3

Semester 2

Course Name	**:**	**ELECTRONIC SYSTEM DESIGN**
Course Code	**:**	**EVR 1104**
Credits	**:**	**3**
L T P	**:**	**2-0-2**

Total No. of Lectures: 28

Total No. of Lab Hours: 28

Course Objectives:

The main objectives of this course are:
1. To introduce the students to the fundamental of Hardware Description Language.
2. To introduce the student to the fundamentals of combinationaland sequential(both synchronous and asynchronous) logic design.
3. To develop an understanding of optimized circuits design and analyze them using various techniques
4. To get acquainted with the concepts of digital system design.

Course Contents

S.No.	Lecture wise breakup	No. of lectures
1	**Design Concepts and Logic Circuits** Digital Hardware, Design Process, Design of Digital Hardware, Basic concepts of Hardware description languages, An overview of VHDL programming: Structural, Data-flow and Behavioural styles, Delay modelling, Control statements, FSM modelling of hardware description language, Datatypes, Operators, Concurrent and Sequential Code, Signal and Variable, Package.	10
2	**Optimized Implementation of Combinational Logic Circuits** Strategy for minimization, Incompletely specified functions, Multiple output circuits, Multilevel synthesis & Analysis. Building Blocks: Multiplexers, Decoders, Encoders Code Converters and their implementation in VHDL, Programmable Logic Devices: PROM, PLA, PAL, FPGA and CPLDs.	6
3	**Synchronous and Asynchronous Sequential Circuits** Synchronous sequential circuits, basic design steps, Mealy state model, Design of FSM and their implementation using VHDL programming. Asynchronous sequential circuits analysis, synthesis, state reduction, state assignment, hazards.	7
4	**Digital System Design** Digital system design, building block circuits, Algorithm state machines: ASM Charts, Pseudo codes, Data-path and control path circuits (Bit counting circuit, Divider, Shift and Add Multiplier etc.), Static timing Analysis, Clock Skew and Clock latency.	5

Lab Work

Sr. No	Lab Module	No. of Hours
1	Simulation and synthesis of Digital circuits with VHDL using Xilinx ISE	10
2	Test vector generation and timing analysis of sequential and combinational logic design realized using VHDL	8
3	Verification of the functionality of designed Digital VLSI circuits using function simulator	8

Course outcomes:

At the completion of this course, students will be able to:	
1	Evaluate and create the PLD based designs using both schematic capture and VHDL
2	Able to perform simulation and synthesis of various combinational and sequential circuits using VHDL
3	Design, build and debug optimized complex combinational circuits
4	Analyze the combinational and sequential circuits based on an abstract functional specification using VHDL.
5	Establish comprehensive understanding of the digital system design

Bibliography:

Sr. No.	Book Detail	Year of Publication
1.	Alan B. Marcovitz," Introduction to Logic Design", Third Edition, McGraw Hill.	2010
2.	Ronald J. Tocci, Neal S. Widmer& Greg Moss, Digital Systems, Global Edition, 12/E,Pearson Education Limited.	2016
3.	Bhaskar, A VHDL Primer, Third Edition, Prentice Hall.	2017
4.	Morris Mano, M. ,Digital Logic and Computer Design, Pearson Education Limited.	2016
5.	Research and review papers in specific area.	

	PO1	PO2	PO3
CO1	2	2	3
CO2	2	2	3
CO3	2	2	3
CO4	2	2	3
CO5	1	1	3

Course Name	**:**	**TESTING & FAULT TOLERANCE**
Course Code	**:**	**EVR1105**
Credits	**:**	**3**
L T P	**:**	**3 0 0**

Total No. of Lectures: 42

Course objectives:

The goal of this subject is to enable students to have the knowledge of

1. Proper detection of faulty chips after manufacturing
2. Test generation for combinational circuits and Design for testability
3. Test generation algorithms for sequential circuits
4. Built in Self test and fault tolerance in VLSI chips.

Course Contents:

S. No.	Course Contents	No. of hrs.
1	**Introduction to Testing:** Introduction to Digital VLSI Testing, Functional and Structural Testing, Structural Testing with Fault Models, Fault Equivalence, Fault Dominance, Fault Collapsing.	04
2	**Fault Simulation**: Fault Simulation, Circuit Simulation, Serial, Deductive, Parallel, and Concurrent Fault Simulation, Critical Path Tracing.	07
3	**Testability Measures:** SCOAP Rules to Compute Combinational Controllability and Observability.	01
4	**ATPG for Combinational Circuits:** ATPG algebra, D- Algorithm, Boolean difference, Path sensitization, Podem, Random, Deterministic and Weighted Random Test Pattern Generation.	07
5	**PLA and Memory Testing:** PLA Testing, Cross Point Fault Model and Test Generation, Memory Testing - Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests.	09
6	**ATPG for Sequential Circuits**: Time Frame Expansion, Scan Chain Based Testing, BILBO, Boundary Scan for Board Level Testing, Built in Self Test and Totally Self checking Circuits.	09
7	**Fault Tolerance:** Introduction to the concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes, Reconfiguration Techniques, Yield Modelling Reliability and Effective Area Utilization.	05

Course outcomes:

At the completion of this course, student will be able to:	
1	Identify the significance of testable design and generate the test pattern for Structure testing.
2	Analyze the fault model, fault coverage and fault simulation.
3	Generate the test patterns for PLA and memory chips.
4	Implement combinational and sequential circuit test generation algorithms.
5	Design the appropriate circuit to embed fault-tolerant techniques.

Books

S. No.	Name of the book/authors/ publisher	Year of publication/reprint
1	Bushnell, M. and Agrawal, V.D., Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits, Kluwer Academic	2000
2	Abramovici M., Breuer M. A. and Friedman A.D., Digital Systems	2001

	Testing and Testable Design, Jaico Publishing House	
3	Pradhan, D.K., Fault Tolerant Computer System Design, Prentice Hall.	1996
4	Research and Review papers in specific area.	-

	PO1	**PO2**	**PO3**
CO1	3	1	3
CO2	2	1	3
CO3	3	1	3
CO4	2	2	3
CO5	3	2	3

Course Name	:	**ANALOG CMOS DESIGN**
Course Code	**:**	**EVR1106**
Credits	**:**	**3**
L T P	**:**	**2-0-2**

Total No. Lectures: 28
Total No. Lab Hours: 28

Course Objectives:

The main objectives of this course are:

1. To understand the principles of analog and mixed-signal IC design in CMOS technologies.
2. To introduce the design of basic analog circuits to provide a foundation for advanced designs.

Course Contents:

Sr.No	Course Contents	No. of Lectures
1.	**Basic MOS Device Physics** MOS VI Characteristics, second order effects, short-Channel effects, MOS device models, review of small signal MOS transistor models, and MOSFET noise, analog layout techniques, symmetry, multi-finger transistors.	**5**
2.	**Analog MOS Process** Analog CMOS process (Double Poly Process), Digital CMOS process tailored to analog IC fabrication, fabrication of active devices, passive devices and interconnects, capacitors and resistors, substrate coupling, ground bounce. Single stage amplifiers: Common source stage, source follower, common gate stage, cascode, Folded cascode.	**5**
3.	**Current Mirrors** Basic Current Mirrors, cascade current mirrors, analysis of current mirrors	**3**
4.	**Differential Amplifier** Single ended and differential operation, qualitative and quantitative analysis of differential pair, common mode response, gilbert cell frequency response of amplifiers: Miller effect, association of poles with nodes, frequency response of all single stage amplifiers. Feedback: general considerations, topologies, effect of loading.	**6**
5.	**Operational Amplifier** General considerations, theory and design, performance parameters, single-stage Op Amps, two-Stage Op Amps, design of 2-stage MOS Operational amplifier, gain boosting, comparison of various topologies, slew rate, offset effects, PSRR. Stability and Frequency Compensation: General Considerations, multi-pole systems, phase margin, frequency compensation, compensation techniques.	**9**

Lab Work:

Sr. No	Lab Module (Credits -1.0)	No. of Hours 28
1.	Familiarization of Cadence Tool (DC and AC transient analysis of CMOS inverter)	4
2.	Use CADENCE Tool to obtain device characteristics of current mirror and single stage amplifier using CMOS	6

3.	Introduction to CADENCE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)	6
4	Simulation of discussed devices using Cadence	6
5.	Projects and case study with the latest tools available in the respective lab.	6

Course Outcomes

At the completion of this course, students will be able to:	
1	Understand the operation of CMOS devices.
2	Understand amplifiers. Basics of MOS device physics, different passive devices and single stage
3.	Understand the basic current mirrors, voltage references, and design basic operational amplifiers.
4.	Understand the concept of gain, power bandwidth.
5.	Design and develop analog circuits using device models.

Bibliography:

Sr.No	Book Details	Year of Publication
1	Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill	2008
2	Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley.	2004
3	Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press, 2nd Edition	2002
4	Johns, D.A. and Martin, K., Analog Integrated Circuit Design, John Wiley	2008
5	Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley, 5th edition	2001
6	Hastings, A., The Art of Analog Layout, Prentice Hall	2005
7	Research and review papers in specific area	

	PO1	**PO2**	**PO3**
CO1	3	1	3
CO2	3	1	3
CO3	3	1	2
CO4	3	1	2
CO5	3	1	3

DEC II

Course Name	:	**Real Time Embedded Systems**
Course Code	**:**	**EVR1251**
Credits	**:**	**3**
L T P	**:**	**2 0 2**

Total No. of Lectures: 28

Total No. of Lab Hours: 28

Course Objectives:

The main objectives of this course are:

1. Describe what makes a system a real time system.
2. Explain the presence of and describe the characteristics of latency in real time systems.
3. Summarize special concerns that real time systems present and how these concerns are addressed..
4. To introduce the students to an exhaustive review of methods for power estimation of digital VLSI subsystems.
5. To understand what makes a system a real time system
6. To understand the characteristics and reasons of latency in real time systems.
7. To describe the real concerns that a real time systems present and how these concerns are addressed.

Sr. No	Course Contents	No. of Lectures
1.	**Introduction:** Issues in real time computing, structure of a real time system. task classes. Characterizing real time Systems and tasks: Introduction, performance measures for real time systems: Traditional performance measures, performability, cost functions and hard deadlines.	**7**
2.	**RTOS and Application design :** Real time operating systems, embedded. RTOS, real time process scheduling, structure of real time operating system, memory management in embedded operating system, operating system, overhead inter-process communication mechanisms, file systems in embedded devices, different types of locks, Semaphores. Real Time Communication: Introduction, architectural issues, protocols: deadlines based protocols, hierarchical round robin protocol, token based protocol.	**6**
3	**Embedded Processing:** Introduction to embedded computing, difference between embedded and general purpose computing, characterizing embedded computing, design philosophies, RISC, CISC, VLIW versus superscalar, VLIW versus DSP Processors, register file design, pipeline design, the control unit, control registers, microprocessor versus microcontroller architecture. Embedded Processors : ARM architecture, assembly programming, input output interfacing, GPIO, LCD interfacing, peripherals, DDR memory, SDRAM, interrupts, timers, Intel atom processor, architecture, application development tools	**8**

4	**System-on-a-Chip (SoC):** System-on-a-Chip (SoC), IP blocks and design reuse, processor cores and SoC, Non-programmable accelerators, reconfigurable logic. Multiprocessing on a chip, symmetric multiprocessing, heterogeneous multiprocessing, in circuit emulation, validation and verification, H/W software partitioning, co-design.	**7**

Lab Work

Sr No.	**Lab Module**	No. of Hours
1.	Develop a project using real time processor	7
2.	Hands on experience on atom boards architecture, application development tools (Hands on Experience on Atom Boards).	7
3.	To program and simulate ARM processor based experiments using flowcode.	7
4.	Case study with the latest tools available in the respective lab.	7

Course Outcomes

At the successful completion of this course, student will be able to:	
1.	Understand the basics and importance of real-time systems
2.	Generate a high-level analysis document based on requirements specifications
3.	Understand basic multi-task scheduling algorithms for periodic, aperiodic, and sporadic tasks as well as understand the impact of the latter two on scheduling.
4.	Identify the unique characteristics of real time systems
5.	Explain the general structure of a real time system
6.	Define the unique design problems and challenges of real time systems

Bibliography:

Sr.No	Book Detail	Year of Publication
1.	Embedded System Design by Santanu Chattopadhya, Second Edition.	2013
2.	Phillip A. Laplante, Real-Time Systems Design and Analysis, Wiley Publishers 4th edition	2011
3.	Lori Matassa, Max Domeika, Break Away with Intel Atom Processors: A Guide to Architecture Migration, Intel Press	2010
4.	Real-Time Systems, Jane W. S. Liu, Pearson Education Asia	2003
5.	Qing Li, Caroline Yao, Real-Time Concepts for Embedded Systems, CRC Press	2003
6.	Research and review papers in specific area.	

	PO1	**PO2**	**PO3**
CO1	3	1	2
CO2	3	1	2
CO3	3	1	3
CO4	3	1	2
CO5	3	1	3
CO6	3	1	3

Course Name	**:**	**VLSI Technology**
Course Code	**:**	**EVR1252**
Credits	**:**	**3**
L T P	**:**	**3-0-0**

Course Objectives:

This course will provide an overview novel VLSI technologies and applications.

1. Learn the fundamentals of VLSI technology and deepen your understanding of them.
2. Develop a grasp of the link between material processing, device fabrication technique, device performance, and intended applications.
3. Understand the fundamental concepts of device integration on different substrates, as well as the benefits and drawbacks of emerging technology that will be employed in future devices.
4. Acquire a basic knowledge of Future Trends in VLSI Technology, as well as the commercialization paths for new materials, methods, and tools for VLSI devices, circuits and Systems.

Unit	Topic	No. of Lecture (42)
1	**Introduction:** History of IC's; Operation & Models for Devices of Interest: CMOS and MEMS, Definition, Need of Clean Room, RCA cleaning of Si.	**3**
2	**Crystal growth:** Source of silicon; Si, Poly Si, Si Crystal Growth, Silicon Wafer Preparation & Crystal Defects.	**4**
3	**Epitaxial Process:** Need of epitaxial layer; vapours phase epitaxy -reactor design, chemistry of epitaxial process, transport mechanism doping & auto doping; selective epitaxy, epitaxial process induced defects, molecular beam epitaxy, merits and demerits among epitaxial processes; recent trends in Epitaxy. **Oxidation:** Dry and Wet Oxidation, Kinetics of Oxidation, Oxidation Rate Constants, Dopant Redistribution, Oxide Charges, Device Isolation, LOCOS, Oxidation System.	**8**
4	**Diffusion:** Pre-Deposition and Drive-in Diffusion Modeling, Dose, 2-Step Diffusions, Successive Diffusion, Lateral Diffusion, Series Resistance, Junction Depth, Irvin's Curves, Diffusion System. **Ion Implantation:** Problems in Thermal Diffusion, Advantages of Ion Implantation, Applications in ICs, Ion Implantation System, Mask, Energy Loss	**6**

	Mechanisms, Depth Profile, Range & Straggle, Lateral Straggle, Dose, Junction Depth, Ion Implantation Damage, Post Implantation Annealing, Ion Channeling, Multi Energy Implantation.	
5	**Lithography:** Basic steps in lithography; lithography techniques-optical lithography, electron beam lithography, x-ray lithography, ion beam lithography; resists and mask preparation of respective lithographies, printing techniques-contact, proximity printing and projection printing; merits and demerits of lithographies; recent trends in lithography at nano regime; **Etching:** Performance metrics of etching; types of etching- wet and dry etching; dry etching techniques-ion beam or ion-milling, sputter ion plasma etching and reactive ion etching (RIE); merits and demerits of etching; etching induced defects; recent trends in etching.	**8**
6	**Thin Film Deposition:** **Physical Vapor Deposition:** Thermal evaporation, Resistive Evaporation, Electron beam evaporation, Laser ablation, Sputtering **Chemical Vapor Deposition:** Advantages and disadvantages of Chemical Vapor deposition (CVD) techniques over PVD techniques, reaction types, Boundaries and Flow, Different kinds of CVD techniques: APCVD, LPCVD, Metallorganic CVD (MOCVD), Plasma Enhanced CVD etc.	**8**
7	**Metallization/Interconnects:** Overview of Interconnects, Contacts, Metal gate/Poly Gate, Metallization, Problems in Aluminum Metal contacts, Al spike, Electromigration, Metal Silicides, Multi-Level Metallization, Planarization, Inter Metal Dielectric.	**5**

Course Outcome:
1. Understand the trends and technologies of VLSI Technology and Semiconductor Road Map for future electronics.
2. Identify the novel materials and material processing techniques for future VLSI devices.
3. Illustrate the different methods involved in VLSI fabrication process. Build the knowledge of process integration-NMOS, CMOS.
4. Assess the various reliability issues in VLSI technology.
5. Understand the fundamental function of micro-nano materials and devices & Describe the various applications of nanotechnology in Communications systems, Energy harvesting, biotechnology & medicine.

Text / Reference Books:

SNo.	Book Details	Edition
1	Fundamentals of Modern VLSI Devices by Yuan Taur & Tak H. Ning (Cambridge)	3rd Edition (2021)
2	Introduction to Nanotechnology Risal Singh & shipra mital gupta (Oxford India Press)	1st Edition (2016)
3	Fundamentals of Microfabrication and Nanotechnology by Marc Madou, (CRC Press)	(3rdEdition)
4	ULSI Technology, Chang, C.Y. and Sze, S.M., (McGraw-Hill)	Latest Edition
5	VLSI Fabrication Principles: Silicon and Gallium Arsenide, S. K. Gandhi, John Wiely and Sons	Latest Edition

CO-PO Mapping:

CO	PO1	PO2	PO3
CO1	**-**	**-**	**2**
CO2	**-**	**-**	**2**
CO3	**-**	**-**	**3**
CO4	**2**	**2**	**3**
CO5	**2**	**-**	**3**

Course Name	**:**	**SEMICONDUCTOR DEVICE MODELING**
Course Code	**:**	**EVR1253**
Credits	**:**	**3**
L T P	**:**	**3-0-0**

Course Objectives:

1. Analyse physical properties of semiconductor materials (carrier concentration and transport, heterojunctions)
2. Evaluate and illustrate the consistency between model and measurement of devices
3. Analyse models for basic device building blocks (pn- junctions, metal-semiconductor contacts and metal-insulator-semiconductor capacitors)
4. Plan and perform modelling and measurements of modern microelectronic devices

Total No. of Lectures: 42

Lecture wise breakup		**No. of Lectures**
1.	SEMICONDUCTOR ELECTRONICS: Physics of Semiconductor Materials, Band Model of Solids, Thermal-Equilibrium Statistics, Carriers in Semiconductors, Drift Velocity, Mobility and Scattering, Drift & Diffusion Current, Hall-Effect	(4)
2.	MODELING BIPOLAR DEVICE PHENOMENA: Injection and Transport Model, Continuity Equation, Diode Small Signal and Large Signal (Charge Control Model), Transistor Models: Ebber – Molls and Gummel Poon Model, Mextram Model, Spice Modeling Temperature and Area Effects.	(6)
3.	FIELD-EFFECT TRANSISTORS (MOSFETs): PHYSICAL EFFECTS AND MODELS: Energy band diagram in equilibrium and under bias, Flat band voltage, Potential Balance and charge balance, Effect of gate body voltage on surface condition, Accumulation and depletion, Inversion, CV Characteristics, Frequency response. Transistor region of operation, Complete all region model, Simplified all region models, Model based on Quasi-Fermi Potential, Regions of inversion in term of terminal voltages, strong inversion, weak inversion, moderate inversion, source referenced vs body referenced modelling, effective mobility, temperature effects.	(8)
4.	Short Channel Effects: Limitation of long channel analysis, short-channel effects: velocity saturation, device degradation, channel length modulation, body bias effect, threshold adjustment, mobility degradation, hot carrier effects, MOSFET scaling goals, gate coupling, velocity overshoot, high field effects in scaled MOSFETs, substrate current and other effects in scaled MOSFETS. Moore law, Technology nodes and ITRS, Physical & Technological Challenges to scaling, nonconventional MOSFET-(FDSOI, SOI, Multi-gate MOSFET)	(8)
5.	Modeling: SPICE transistor modeling, compact MOSFET modeling approaches, history of BSIM models, MOS Transistors: LEVEL 1, LEVEL 2 ,LEVEL 3, BSIM, HISIMVEKV Models, Threshold voltage modeling. Punch through. Carrier velocity modeling. Short channel effects. Channel length modulation. Barrier lowering, Hot carrier effects. Mobility modeling, Model parameters; Analytical and Numerical modeling of BJT and MOS transistors.	(8)

6	Numerical Simulation: Numerical simulation, basic concepts of simulations, grids, device simulation and challenges. Importance of semiconductor device simulators - Key elements of physical device simulation, historical development of the physical device modeling. Introduction to the TCAD Simulation Tool, Examples of TCAD Simulations – MOSFETs and SOI	(8)

Course Outcomes: By the end of this course, the students will be able to	
1.	To introduce the physics of semiconductor materials for understanding the device modelling of semiconductor devices.
2.	To understand the transport of charge carriers for the operation of semiconductor devices.
3.	To apply suitable approximations and techniques to derive the physical model of semiconductor devices such as P-N junctions
4	To analyze electrostatic variables and current-voltage characteristics of MOS devices under a variety of conditions.
5	To evaluate qualitative understanding of the physics of emerging MOS devices and conversion of this understanding into modeling.
6	To develop the fundamental understanding of device modeling and numerical simulation and prepare report on it.

Suggested Books:		
Sr. No.	**Name of Book/Authors/Publisher**	**Year of Publication /Reprint**
1	Advanced Semiconductor Devices by Taur and Ning.	**Latest Edition**
2	Device Electronics for Integrated circuits by Muller and Kammins	**Latest Edition**
3	Computational Electronics: Semiclassical and Quantum Device Modeling and Simulation by Dr. Vagica Vasileska and Stephen M. Goodnick	**Latest Edition**
4	Semiconductor Device Modelling by A B. Bhattacharyya	**Latest Edition**
References		
1. Physics of Semiconductor Devices by S. M. Sze and Kwok K. Ng, 3rd Edition, (John Wiley & Sons, 2002). 2. Semiconductor Device Fundamentals by Robert F. Pierret, Addison-Wesley Publishing, 1996. 3. Semiconductor Physics and Devices by Donald A. Neamen, 3rd Edition, Mc Graw Hill, 2003 4. Semiconductor Devices- Basic Principles", by Jasprit Singh, John Wiley and Sons Inc., 2001		

CO	PO1	PO2	PO3
CO1	-	-	2
CO2	-	-	2
CO3	-	-	3
CO4	2	-	3
CO5	2	-	3
CO6	2	2	3

Course Name	**:**	**Optoelectronic materials and devices**
Course Code	**:**	**EVR1254**
Credits	**:**	**3**
L T P	**:**	**3-0-0**
Course Objective: The course on optical electronic materials and devices explains the various materials and their optoelectronic properties , nanophotonic materials . Other latest aspects that will be dealt are display technologies and solar cells .		

		Total No. of Lectures - 42
Lecture wise breakup		**No. of Lectures**
1.	**Optical properties** of semiconductors, Dielectrics and polymers; Ray optics, Electromagnetic optics and guided wave optics; Physics of light-matter interactions; Photoactive polymers- Radiation sensitive resisters, Optical properties of σ- and π-conjugated polymers, Relaxation process in organic polymer systems, Light emission in polymers, Polymeric materials for nonlinear optical properties- photorefractive polymers, polymers with high two photon activities, optical phase change materials and meta optics, 2D material photonic integration	(11)
2.	**Nano Photonics:** Photons and electrons similarities and differences- Confinement of photons and electrons, Propagation through classically forbidden zone: tunneling, Nano scale optical interactions, Nano scale confinement of electronic interactions -quantum confinement effect. Nano crystals and quantum confined materials. Quantum confined structures as lasing media and super lattice; Optical properties, Metallic nanoparticles and Nanorods Applications of Metallic nano structures.	(11)
3	DISPLAY DEVICES AND LASERS Introduction, Photo Luminescence, Cathode Luminescence, Electro Luminescence, Injection Luminescence, Injection Luminescence, LED, Plasma Display, Liquid Crystal Displays, Numeric Displays	(10)
4.	Device Physics of Solar Cells, Principle of solar energy conversion, Conversion efficiency, Single, Tandem multi-junction solar cells , Principle of cell design , Crystalline silicon and III-V solar cells ,Thin film solar cells: Amorphous silicon ,Quantum Dot solar cells, Introduction to Dye Sensitized Solar Cells and Organic Solar Cells, Perovskite Solar Cells, Nanomaterials for Photovoltaic	(10)

Course Outcomes: By the end of the course, the student must be able to:	
1	To understand different light modulation techniques and the concepts and applications of optical switching.
2	Understand the optoelectronic properties of the material , light matter interaction at micro and nanoscale .
3	Explore the latest materials to be used for various applications in the optical domain such as solar cells, displays and sensors etc.
4	Illustrate the working principles and physics of display devices and solar cells.

5	Understand and Analyse the integration process and application of opto electronic integrated circuits in transmitters and receivers.

Suggested Books:		
Sr. No.	**Name of Book/ Authors/ Publisher**	**Year of Publication/ Reprint**
1	C.P. Wong, Polymers for Electronic and Photonic Applications, Academic Press, 1993.	Latest Edition
2	S.O. Kasap, P. Capper, Handbook of Electronic and Photonic Materials, Springer, 2006.	Latest Edition
3	A. Yariv and P. Yeh, "*Photonics*," 6th ed, Oxford, 2007.	2007
4	S.O. Kasap, Optoelectronics and Photonics: Principles and Practices, Pearson Education, 2009	2009
5	Nano Photonics; P N Prasad Wiley Interscience (2003)	Latest edition
6	Semiconductor optoelectronic devices: Pallab Bhattacharya, Pearson(2008).	Latest Edition
7	Optoelectronics: An introduction to materials and devices, Jasprit Singh, Mc Graw Hill International Edn., (1996).	Latest Edition
8	Wenham, S., M. Green, et al., eds. *Applied Photovoltaics*. 2nd ed. Routledge, 2006. ISBN: 9781844074013	Latest Edition
9	Luque, A., and S. Hegedus, eds. *Handbook of Photovoltaic Science and Engineering*. John Wiley & Sons, Ltd, 2003. ISBN: 9780471491965	Latest Edition

CO-PO Mapping:

CO	**PO1**	**PO2**	**PO3**
CO1	**-**	**-**	**3**
CO2	**2**	**-**	**3**
CO3	**-**	**-**	**3**
CO4	**-**	**-**	**3**
CO5	**2**	**1**	**3**

Open Electives

Course Name	**:**	**NEURAL NETWORKS :**
Course Code	**:**	**EVR 3001**
Credits	**:**	**3**
L T P	**:**	**3-0-0**

Course Objectives:

The goals of this course are

1. To introduce some of the fundamental techniques and principles of neural computation.
2. Basic neural network models, single and multilayer perceptron.
3. To investigate some associative Networks
4. To introduce some of neural networks based on competition.

Total No. of Lectures: 42

	Course Contents	**No. of Lectures**
1.	**Introduction to neural networks**: Introduction to artificial neural networks, biological neural networks, comparison between biological and artificial Neural Networks, terminology and various architectures of Neural Networks, History of Neural Networks.	3
2.	**Fundamental concepts:** MC Culloch-Pitt Neuron model, various Activation functions, Hebbnet, Biases and threshold, Linear separability.	4
3.	**Pattern Classification:** Perceptron, Adaline and Madaline. Architecture, training algorithms and application algorithms of these networks, practical implementation using matlab.	7
4.	**Pattern Association:** Architecture, Training and application Algorithms for Pattern Association networks, Heteroassociative Memory Neural Network, Auto associative Net, Iterative Auto associative Net, Bidirectional Associative Memory, Discrete Hopfield Network, practical implementation of these networks using matlab.	7
5.	**Competitive Nets:** Maxnet, Mexican Hat, Hamming Net, Kohonen Self Organizing Maps, Learning Vector Quantization, Full and Forward Counterpropagation. Application based on these networks. Use of Counterpropagation net for a mathematical function, practical implementation using matlab.	7
6.	**Adaptive and Backpropagation networks:** Adaptive Resonance Theory: Introduction, architecture, algorithm and application of ART1. Backpropagation neural net, architecture, algorithm, variations, applications, derivation of learning rules. Applications based on backpropagation neural net.	7
7.	**Fixed Weight Networks**: Fixed-Weight Nets for Constrained Optimization, Neural Net approach to Constrained Optimization, Boltzmann Machine: architecture, algorithm, Travelling Salesman Problem. Examples based on Boltzmann Machine.	7

Course Outcomes: Upon successful completion of this course, the enrolled students will be able

to	
1.	Implement neural networks for pattern classification.
2.	Adequate knowledge about activation functions used for neural networks.
3.	Design a fault tolerant neural network for character recognition.
4.	Application of neural networks to generate functions.
5.	Design multi-layered neural networks to solve complex problems.
6.	Solve complex problems using fixed weight neural networks like Travelling Salesman Problem.

Bibliography:

S. No.	Name of the book/authors/ publisher	Year of publication/reprint
1.	Fundamentals of Neural Networks, Laurence Fausett, Pearson Education	2006
2.	Neural networks and Fuzzy Logic, K Vinod Kumar, R. Saravana Kumar, Katson Books	2012
3.	Neural Networks and machine learning, Haykin, Pearson Education	2008
4.	Neural Networks, Satish Kumar, TMH	2001
5.	Introduction to Neural Networks using MATLAB 6.0,S. N. Sivanandam, S. Sumathi and S.N. Deepa, Mc Graw Hill	2006

	PO1	**PO2**	**PO3**
CO1	2	1	2
CO2	2	1	2
CO3	3	1	3
CO4	3	1	2
CO5	3	1	3
CO6	2	1	3

Course Name	**:**	**Flexible Electronics : Materials and Circuits**
Course Code		**EVR3002**
Credits	**:**	**3**
L T P	**:**	**3-0-0**

Course Objectives:

Gain a fundamental understanding of the field of organic and printed electronic materials, fabrication techniques and devices and their potential impact.

1. Learn the fundamentals of flexible and printable electronics and deepen your understanding of them.
2. Develop a grasp of the link between soft matter electronics printing techniques, device performance, and intended applications.
3. Understand the fundamental concepts of device integration on flexible platforms, as well as the benefits and drawbacks of emerging technology that will be employed in future devices.
4. Acquire a basic knowledge of Future Trends in Flexible/Printable Electronics Technology, as well as the commercialization paths for new materials, methods, and tools for printed and flexible electronic systems.

Total No. of Lectures: 42

	Lecture Wise Breakup	**No. of Lecture**
1	Motivation for study of organic and printed flexible electronics	**2**
2	Materials properties/synthesis of printable semiconductors: Nanowire and nanoparticle synthesis, transition metal oxides, amorphous thin films, polymeric semiconductors, structure and property relationships, paper-based electronics, textile substrates, barrier materials.	**5**
3	Thin-film Deposition and Processing Methods for Flexible: Devices CVD, PECVD, PVD, etching, photolithography, low-temperature process integration	**3**
4	Introduction: display and lighting technology, solar cells and sensors	**12**
5	Organic and Printable Flexible Electronics (Flexible displays technologies, Flat panel lighting technologies, Flexible solar cells and Flexible electronics for RF applications)	**8**
6	Thin Film Transistors: Thin Film Thin Film Transistors device structure and performance. Fundamental issues for low-temperature processing, Low temperature thin-film transistor Devices, Device structures and materials processing, Low-temperature a-Si:H and a-IGZO thin-film transistor device performance, I-V characteristics, device stability.	**6**
7	Organic sensors (bio & chemical): Organic material synthesis and Deposition techniques, challenges and road block in fabrication and development of flexible and organic electronics devices.	**6**

Course Outcome:

1. Understand the trends and technologies of flexible electronics and its road map.
2. Identify the materials used in the design and manufacturing of flexible electronic devices.
3. Recognize and introduce the various thin-film deposition techniques used in fabrication of Flexible and Printable electronics devices.

4.	To provide an understanding of the structure and features of TFT devices.
5.	Develop an ability to design a system, component, or process to meet desired needs using novel materials and devices.

Text / Reference book:

1. Wong, William S., Salleo, Alberto, Flexible Electronics: Materials and Application, https://doi.org/10.1007/978-0-387-74363-9.
2. Guozhen Shen and Zhiyong Fan, Editors, Flexible Electronics: From Materials to Devices, MRS Bulletin 41, 818–819 (2016). https://doi.org/10.1557/mrs.2016.227
3. Zhenan Bao and Jason Locklin, Organic Field-Effect Transistors (Optical Science and Engineering), CRC Press, 2007
4. Ioannis Kymissis, Organic Field-Effect Transistors: Theory, Fabrication and Characterization (Integrated Circuits and Systems), Springer, 2009
5. Qiquan Qiao (Editor), Organic Solar Cells: Materials, Devices, Interfaces, and Modeling (Devices, Circuits, and Systems), CRC Press, 2015
6. Christoph Brabec, Ullrich Scherf, Vladimir Dyakonov (Editors), Organic Photovoltaics: Materials, Device Physics, and Manufacturing Technologies, Wiley-VCH, 2014
7. Frederik C. Krebs, Stability and Degradation of Organic and Polymer Solar Cells, Wiley, 2012
8. Hagen Klauk (Editor), Organic Electronics: Materials, Manufacturing, and Applications, Wiley-VCH, 2006; Organic Electronics II: More Materials and Applications, Wiley-VCH, 2012
9. Franky So (Editor), Organic Electronics: Materials, Processing, Devices and Applications, CRC Press, 2009
10. Mario Pagliaro, Flexible Solar Cells, Wiley-VCH, 2008.

CO-PO Mapping:

CO	PO1	PO2	PO3
CO1	**-**	**-**	**3**
CO2	**2**	**-**	**3**
CO3	**-**	**-**	**3**
CO4	**-**	**-**	**3**
CO5	**2**	**1**	**3**

Course Name	**:**	**Neuromorphic Engineering**
Course Code	**:**	**EVR3003**
Credits	**:**	**3**
L T P	**:**	**3-0-0**

Course Objectives:

To provide an insight of neuromorphic electronic devices, circuits and system design.

1. Learn Ultra-low power computing electronics concepts mimicking computing by biological neurons.
2. Develop a grasp of different Design and simulation techniques of CMOS and nano electronic circuits modelling biological brain.
3. Understand Commercial neuromorphic systems and processors for machine learning applications.
4. Acquire a basic knowledge of Future Trends in neuromorphic engineering Technology, as well as the commercialization paths for new materials, methods, and tools for neuromorphic electronic systems design.

	Total number of Lectures-42	
Lecture wise breakup		**No. of Lecture**
1	Introduction to classic neuromorphic circuits. Signalling and operation of Biological neurons, neuron models, signal encoding and statistics; Synapses and plasticity rules, biological neural circuits.	**8**
		5
2	MOSFETs for Neuromorphic electronics : FETs - device physics and sub-threshold circuits.	**6**
3	Analog and digital electronic neuron design.	**6**
4	Programmable Neuromorphic Circuits and Synapses: (Spiking Neural Network, Non-volatile memristive semiconductor devices; Electronic synapse design; Interconnection Networks; Interconnection schemes for large non-spiking and spiking neural networks).	**12**
5	Analog and Digital Neuromorphic Circuit and System Design: Analysis of design, architecture and performance characteristics of demonstrated chips employing Analog neuromorphic and Digital neuromorphic VLSI, Electronic synapses and other neuromorphic systems.	**10**

Course Outcome:

1. Build power-saving hardware devices to analyse real-world noisy data utilizing brain-like mechanisms.
2. Identify and learn basic concepts and current trends in neuromorphic device, circuit, and system design.
3. Design, Develop and Document Analog and Digital neuromorphic systems.
4. Apply neuromorphic systems to develop new VLSI circuits and make report on the same.

5. The students will learn how electronics circuits mimic biological neurons, and will explore their novel variations in these circuits.

Text/Reference book:
1. Shih-Chii Liu, Jörg Kramer, Giacomo Indiveri, Tobias Delbrück, Rodney Douglas, **Analog VLSI: circuits and principles**, MIT press, 2002, ISBN 0262122553
2. Carver Mead, **Analog VLSI and neural systems**, Addison-Wesley, 1989, ISBN0201059924
3. Eric Kandel, James Schwartz, Thomas Jessell, Steven Siegelbaum, A.J. Hudspeth, **Principles of neural science**, McGraw Hill 2012, ISBN 0071390111
4. **Dale Purves, Neuroscience**, Sinauer, 2008, ISBN 0878936971

CO-PO Mapping:

CO	PO1	PO2	PO3
CO1	**-**	**-**	**3**
CO2	**-**	**-**	**3**
CO3	**2**	**3**	**3**
CO4	**2**	**3**	**3**
CO5	**2**	**-**	**3**

Course Name	**:**	**SENSORS AND ACTUATORS**
Course Code	**:**	**EVR3004**
Credits	**:**	**3**
L T P	**:**	**3-0-0**

Course Objectives:

By the end of this course, the students will be able to:

1. Understand sensors, how to fabricate the sensors and its application in real world.
2. Design modern day microsensors and micro actuators
3. Create sensor modules in EDA/TCAD tools simulate them for correct operations before fabricating it.

Total No. of Lectures: 42

Lecture wise breakup		**No. of Lectures**
1.	Basics of Energy Transformation, Transducers, Sensors and Actuators	(3)
2.	Thin film physics, Application in MOSFET and its variants	(4)
3.	Thin Film Deposition Techniques: Chemical Vapor Deposition (APCVD, LPCVD, UHVCVD, PECVD, ALCVD, HPCVD, MOCVD) , Physical Vapor Deposition (Thermal Deposition, E-beam Evaporation, Sputtering, Pulsed Laser Deposition), Basic understanding of Photolithography for pattering layer. Detailed overview of Etching methods.	(6)
4.	Gas sensors: Optical gas sensor, Metal oxide semiconductor gas sensor, Field effect transistor gas sensor, Piezoelectric gas sensor, Polymer gas sensor, Nano-structured based gas sensors, Design and fabrication process of Microsensors: Force Sensors, Pressure Sensors, Strain gauges and practical applications	(8)
5.	Actuators: Piezoelectric and Piezoresistive actuators, micropumps and micro actuators with practical applications , basics of microfluidics to assist Photomask design using Clewin Software, pattern transfer techniques, PDMS moulding and degassing, device bonding techniques.	(8)
6	Interfacing: Sensor Interfacing with Microprocessor to build electronic system, Static and Dynamic Characteristic Parameters for Sensors and Actuators, Calibration of Sensor based electronics systems	(8)
7	Static and Dynamic Characteristic Parameters for Sensors and Actuators, Calibration of Sensor based electronics systems	(5)

Course Outcomes: By the end of this course, the students will be able to	
1.	Explain fundamental physical and technical base of sensors and actuators
2.	Describe basic laws and phenomena that define behaviour of sensors and actuators,
3.	Analyse various premises, approaches, procedures and results related to sensors and actuators,
4.	Create analytical design and development solutions for sensors and actuators and present a report of the same.
5.	Understand the functions of sensors, actuators and associated control systems for real time applications.

Suggested Books:

Sr. No.	**Name of Book/Authors/Publisher**	**Year of Publication /Reprint**

1.	Sensors and Signal Conditioning Wiley-Blackwell	2008
2	Jacob Fraden, Handbook of modern sensors, Springer, Stefan Johann Rupitsch.	Latest edition
3	Piezoelectric Sensors and Actuators: Fundamentals and Applications, Springer, 2018 Senturia S. D.	2018
4.	Microsystem Design, Kluwer Academic Publisher, 2001 J.D. Plummer, M.D. Deal, P.G. Griffin	2001
5.	Silicon VLSI Technology, Pearson Education, 2001 S.M. Sze (Ed)	2001
6.	VLSI Technology, 2nd Edition, McGraw Hill, 1988 Madou	Latest edition
7.	M Fundamentals of Microfabrication, CRC Press, 1997.	Latest edition

CO	PO1	PO2	PO3
CO1	**-**	**-**	**3**
CO2	**-**	**-**	**3**
CO3	**1**	**-**	**3**
CO4	**2**	**3**	**3**
CO5	**2**	**2**	**3**